Next Generation 인터페이스 테크놀로지 트렌드

(USB3.1, HDMI2.0, MHL3.2)

텍트로닉스
박영준 부장

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Agenda

- USB3.1 Compliance Test update
  - What's different for USB3.1
  - Transmitter and Receiver Compliance Test
- HDMI2.0, MHL3.2 overview
- Q & A

What's different for USB3.1

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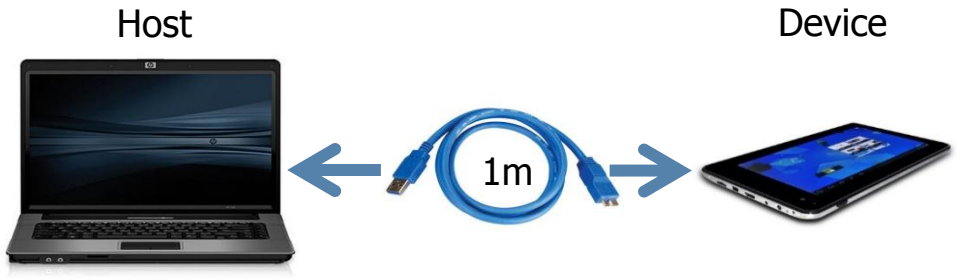
USB 3.1 Comparison

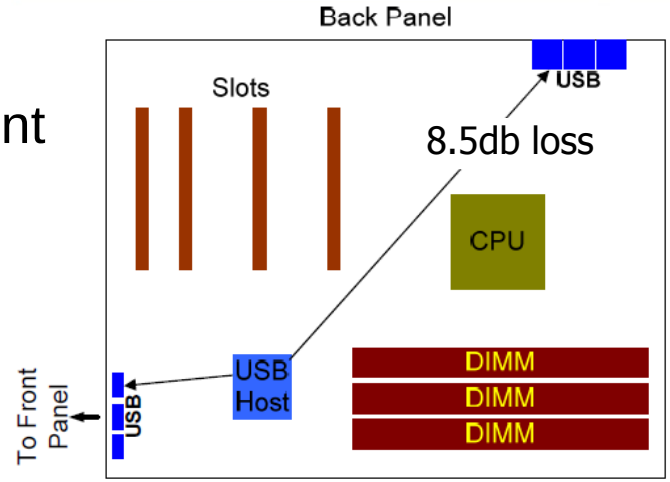
	Gen1	Gen2
Data Rate	5 Gb/s	10 Gb/s
Encoding	8b/10b	128b/132b
Target Channel	3m + Host/ Device channels (-17dB, 2.5 GHz)	1m + board ref channels (-23dB, 5 GHz)
LTSSM	LFPS, TSEQ, TS1, TS2	LFPSPlus, SCD, TSEQ, TS1, TS2,
Reference Tx EQ	De-emphasis	3-tap (Preshoot/De-emphasis)
Reference Rx EQ	CTLE	CTLE(6 level) + 1-tap DFE
JTF Bandwidth	4.9 MHz	7.5 MHz
Eye Height (TP1)	100 mV	70 mV
TJ@BER	132 ps (0.66 UI)	71 ps (0.714 UI)
Backwards Compatibility	Y	Y
Connector	Std A	Improved Std A with insertion detect

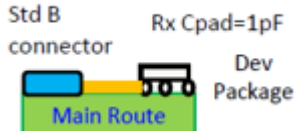
* SCD: Speed Capability Declaration

USB 3.1 Key Considerations – Long Channel

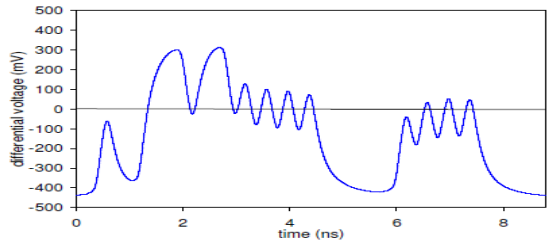
- Channel characteristics
  - 8.5dB loss host PCB route
  - 8.5dB loss device PCB route
  - 1m cable
- Cause Frequency dependent loss (ISI) and Crosstalk
- Close the 10Gb/s eye

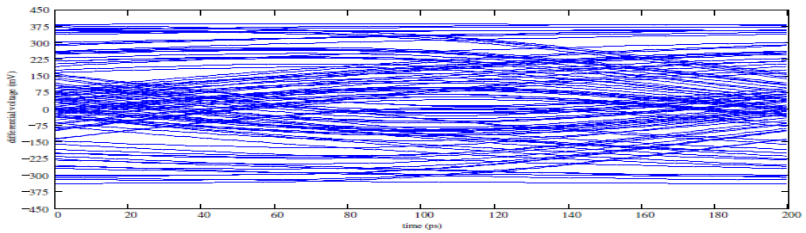






8.5db loss





Source: USB DevCon

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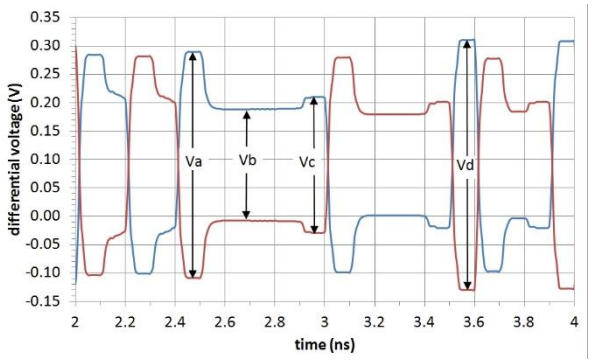
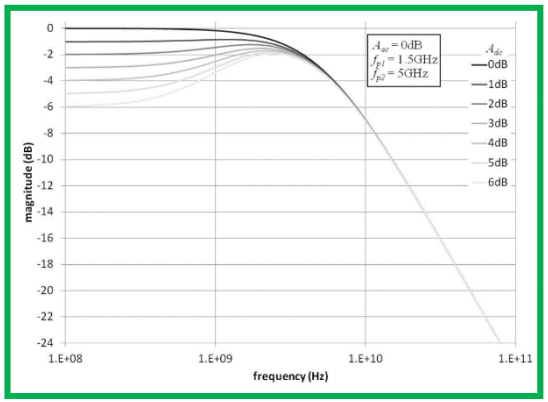
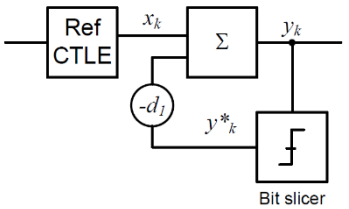
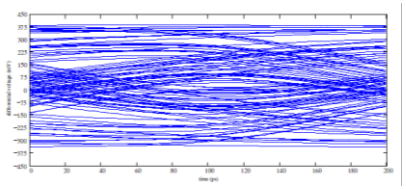
USB 3.1 Key Considerations – TX,RX Equalization

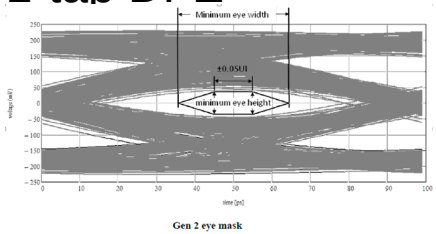






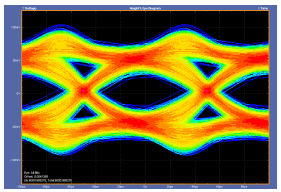
- Transmitter Equalization
  - 2.2 dB Preshoot
  - -3.1 dB De-emphasis
- Receiver Equalization
  - multiple CTLE gain settings
  - 1-tap DFE





Gen 2 eye mask

- Enable to open Receiver eye



CTLE

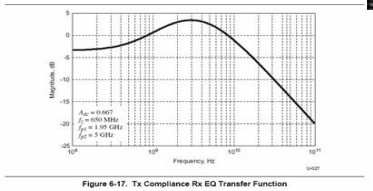


Figure 6-17. Tx Compliance Rx EQ Transfer Function

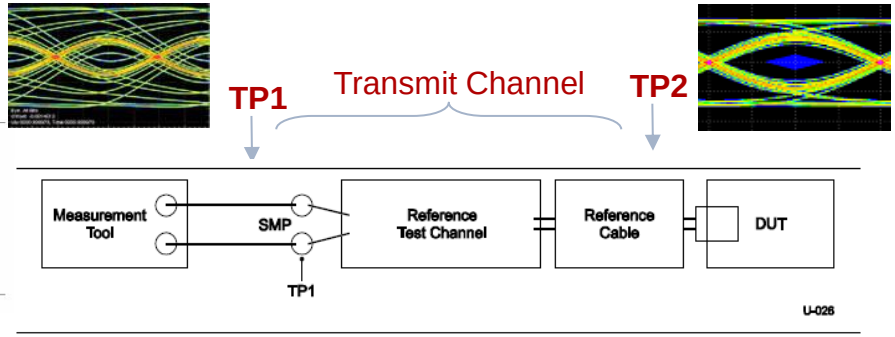


Figure 6-19. Tx Normative Setup with Reference Channel

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Source: USB DevCon

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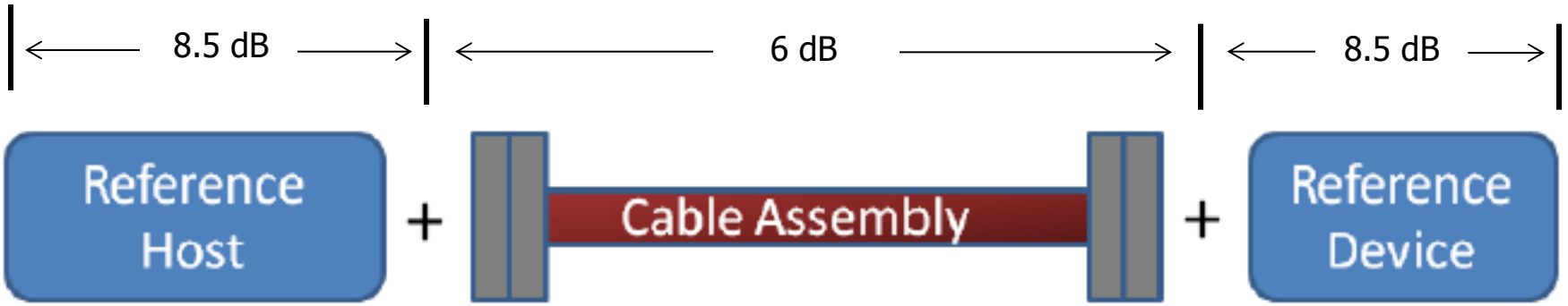
New Channel Budget of USB3.1

- Target 23 dB @ 5 GHz loss budget (die-to-die)
- Equal channel allocation for host/device
- Tx EQ settings recommended (normative)
  - 2.2 dB Preshoot and -3.1 dB De-emphasis
  - Requires additional compliance patterns for Tx testing
- Host or device loss that exceeds 8.5dB may required repeater
  - Need end-to-end training -> link aware repeaters



* Items in red indicate new as Aug 2014 release

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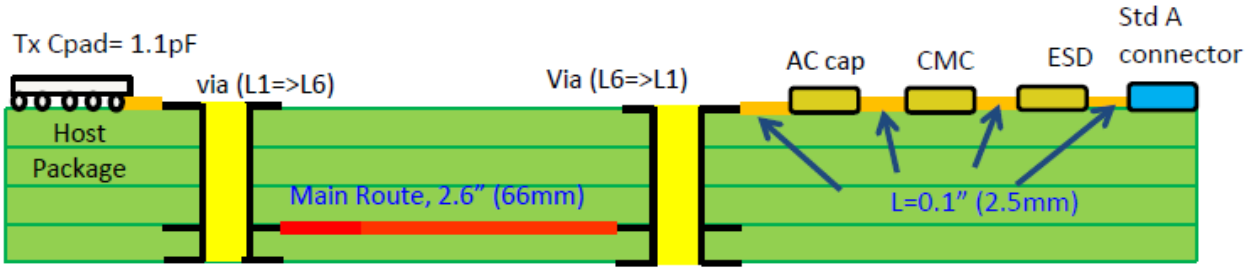
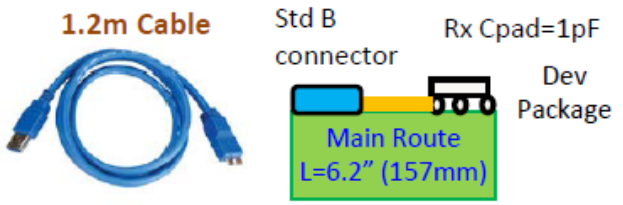
23 dB Reference Channel Loss

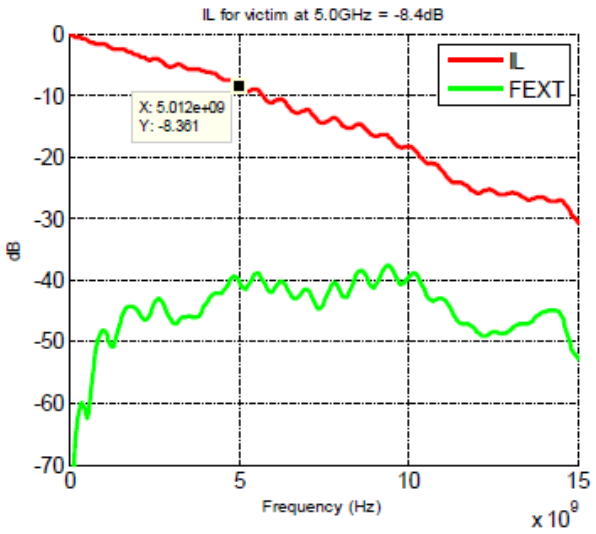
Host (Type 3 PCB)



Dev (Type 3 PCB)

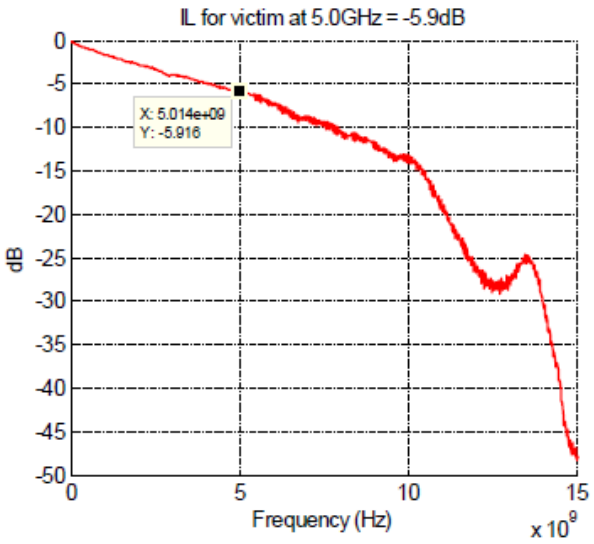


8.5dB Host

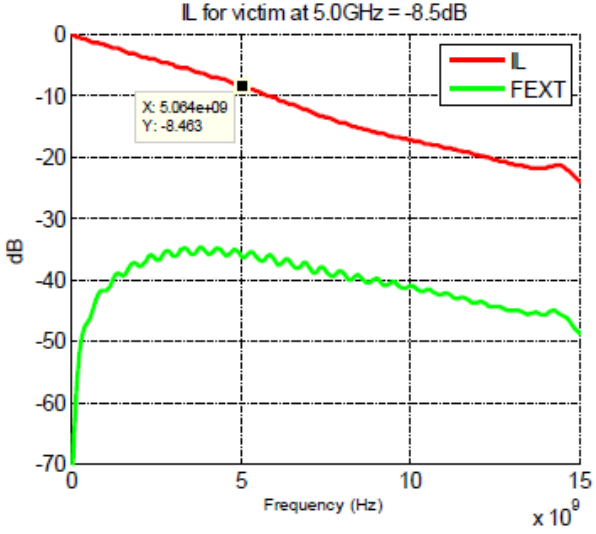


6dB Cable

(with mated connectors)



8.5dB Device



Source: USB-IF Developer Training

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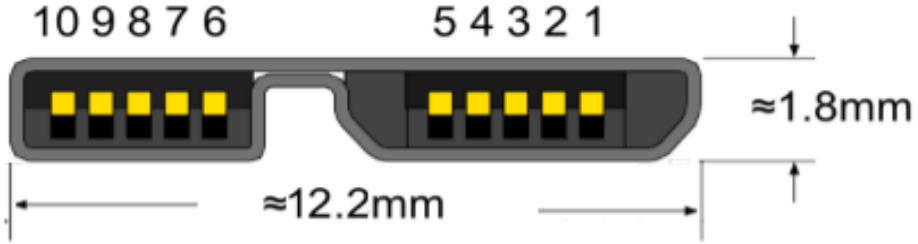
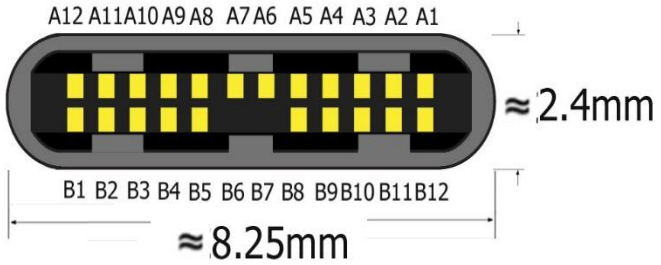
Type-C Comparison

- Rounded, reversible, flip-able
- ~25% less width vs.µB
- Signaling
  - Two SS differential pairs
  - Vbus power
  - Configuration Channel (CC)
  - USB 2.0 differential pair
  - Plug power (Vconn)

Micro B Plug



Type-C Plug



A1	A2	A3	A4	A5	A6	A7	A8	A9	A10	A11	A12
GND	TX1+	TX1-	VBUS	CC	D+	D-	SBU1	VBUS	RX2-	RX2+	GND
GND	RX1+	RX1-	VBUS	SBU2			VCONN	VBUS	TX2-	TX2+	GND
B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1

* New signals

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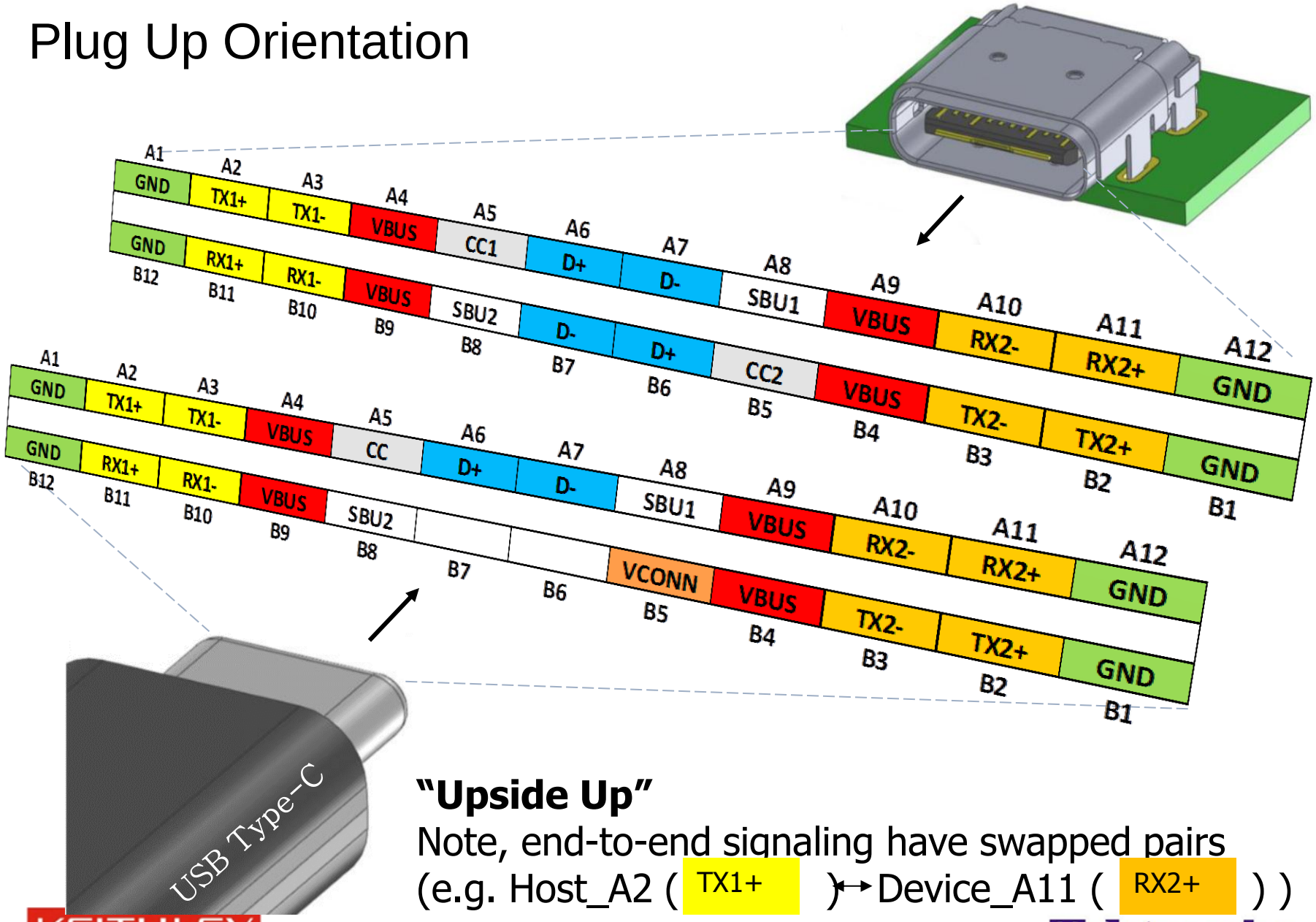
Plug Up Orientation



"Upside Up"

Note, end-to-end signaling have swapped pairs

(e.g. Host_A2 (TX1+) ↔ Device_A11 (RX2+))

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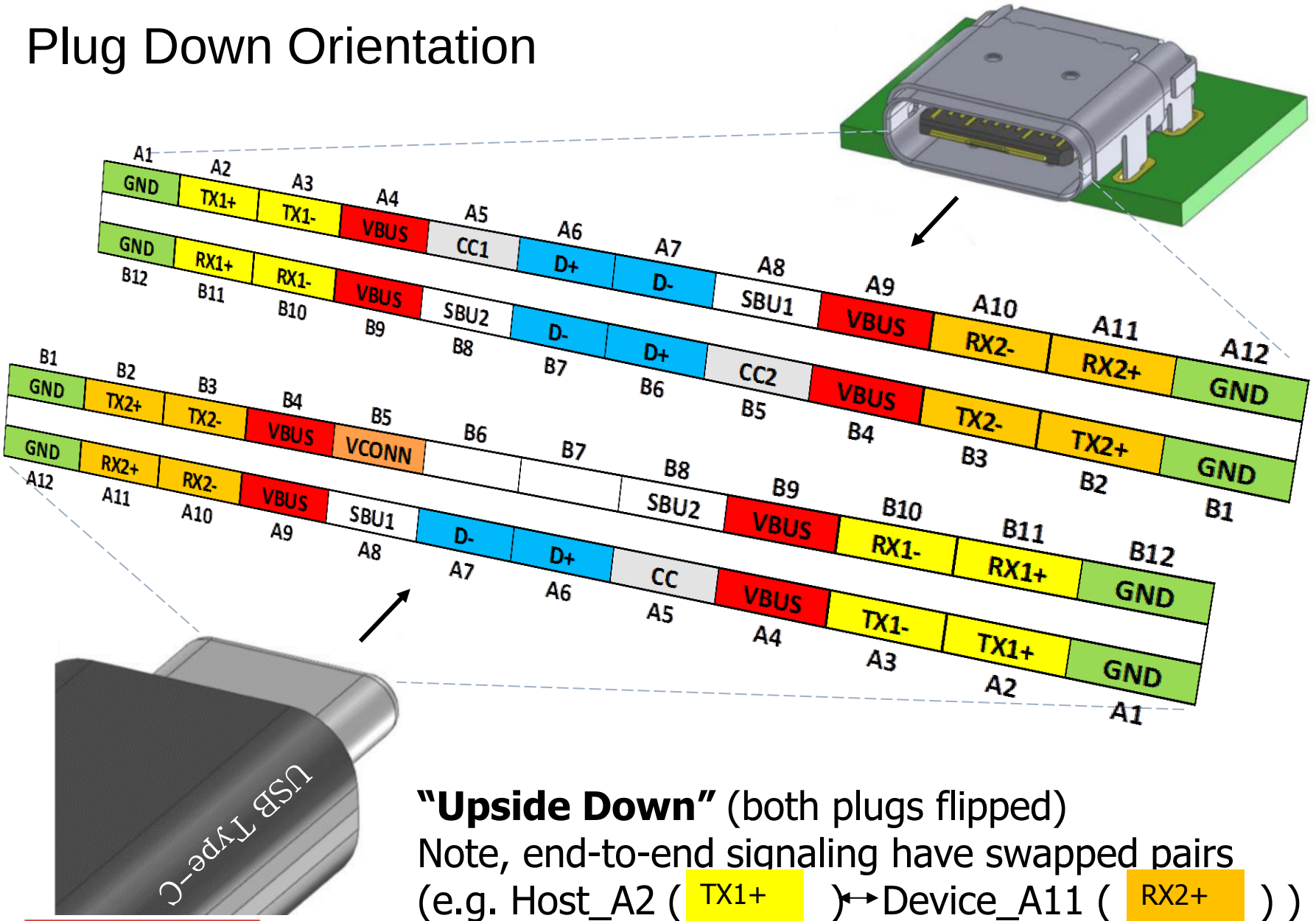
Plug Down Orientation



"Upside Down" (both plugs flipped)
Note, end-to-end signaling have swapped pairs
(e.g. Host_A2 (TX1+) ↔ Device_A11 (RX2+))

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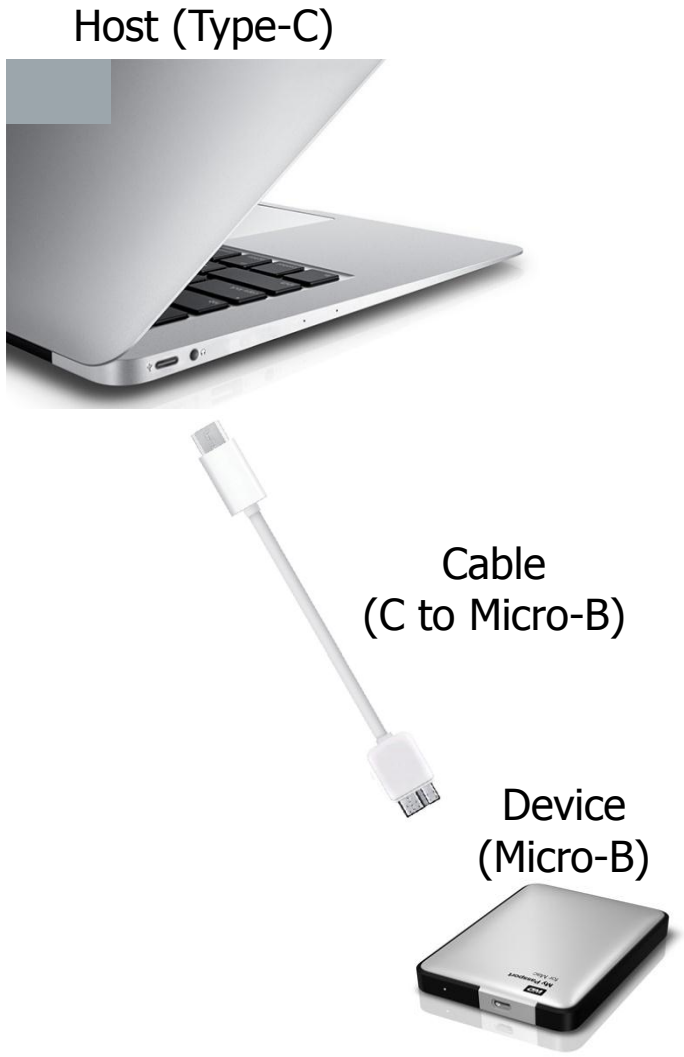
Connector Transition

Legacy Cables

Plug 1	Plug 2	Version	Length
A	C	USB 2.0	≤ 4m
A	C	USB 3.1 Gen2	≤ 1m
C	B	USB 2.0	≤ 4m
C	B	USB 3.1 Gen2	≤ 1m
C	Micro-B	USB 2.0	≤ 2m
C	Micro-B	USB 3.1 Gen2	≤ 1m

Defined Adapters

Plug 1	Plug 2	Version	Length
C	Micro-B	USB 2.0	≤ 0.15 m
C	A	USB 3.1 Gen1	≤ 0.15 m



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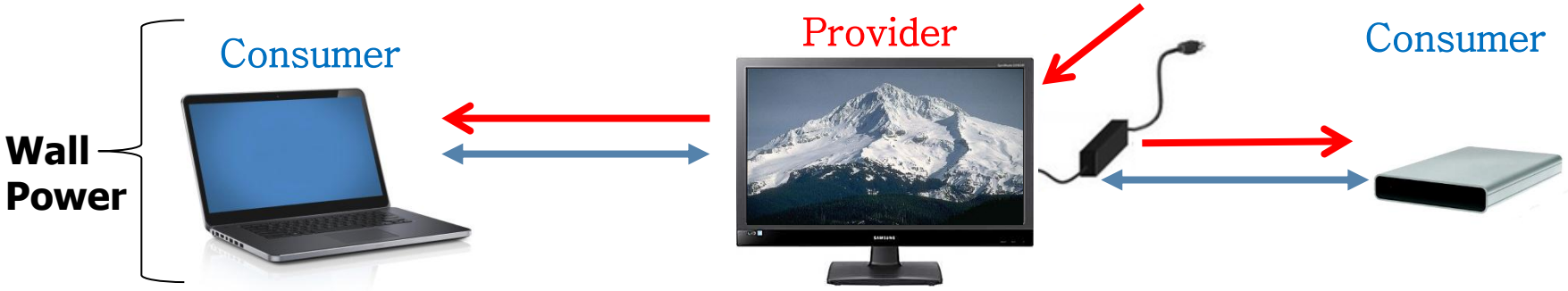
USB Power

- **USB 3.0** power handling -> Up to 900 mA (Nov 2008)
- **Battery Charging** (BC 1.2, Dec 2010)
  - Increases charging of up to 1.5 A
  - No simultaneous data transfer in high power mode
- **Power Delivery** (PD 2.0, August 2014) specification
  - Up to 100W with switchable power delivery source
  - Switchable power delivery source without changing cable direction



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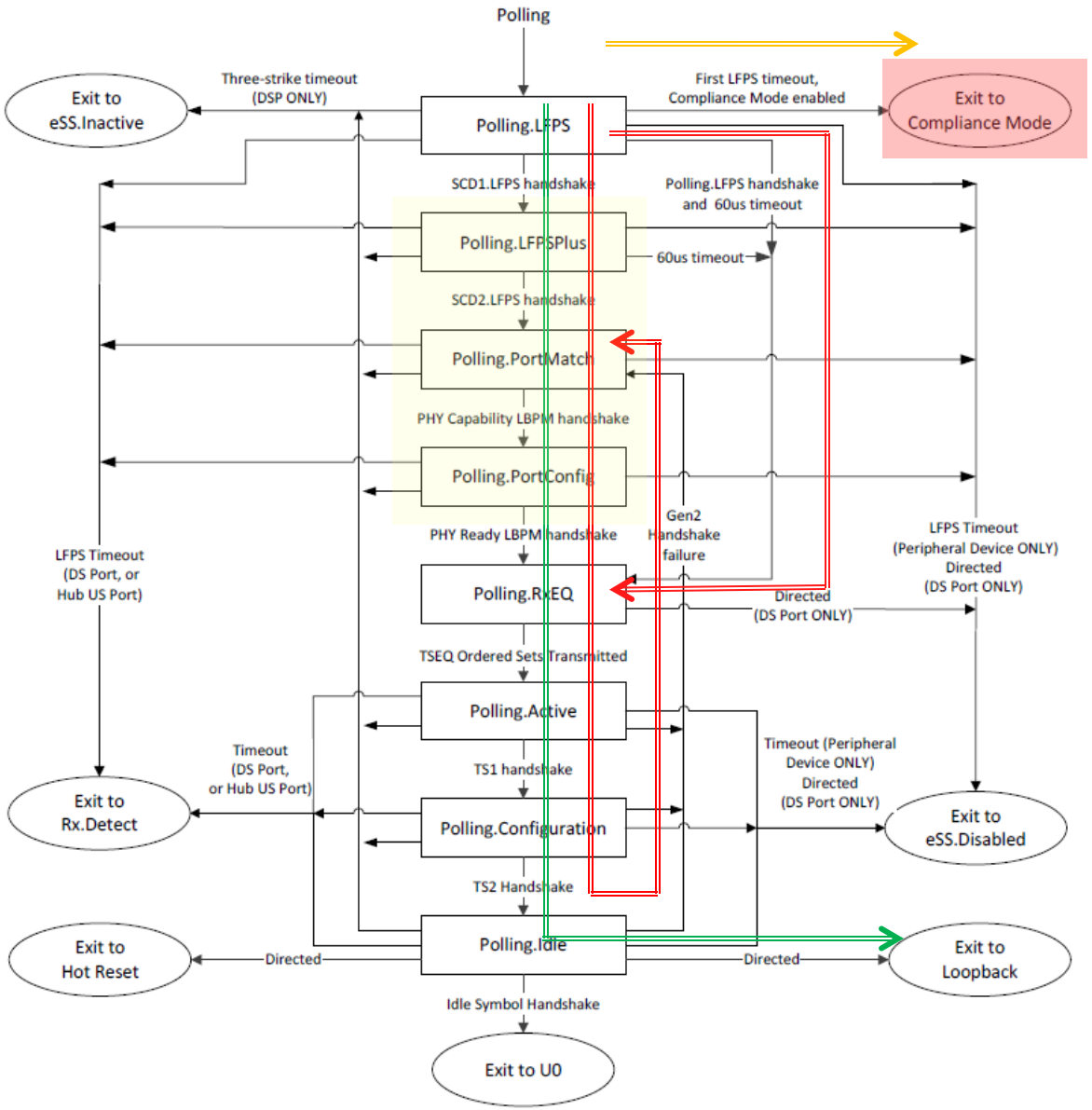
Transmitter Compliance Test

Entering to Compliance Mode for Transmitter test –Compliance TX



Successful Gen2 link training with loopback asserted – Enter in Loopback mode

No link partner response – Enter Tx compliance mode

Training failure – Retry at Gen1 rate

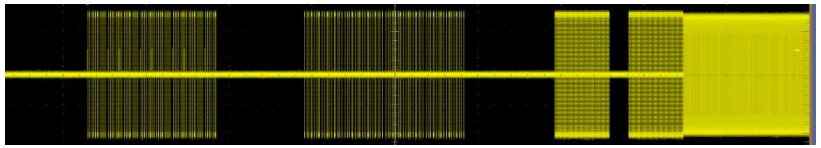
LFPS detected but no LFPSPlus - Train at Gen1 rate

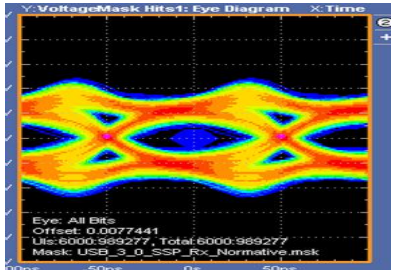
USB3.1 Transmitter Compliance Testing Patterns

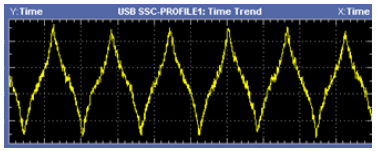
Table 6-13. Compliance Pattern Sequences

Compliance Pattern	Value	Description
CP0	D0.0 scrambled	A pseudo-random data pattern that is exactly the same as logical idle (refer to Chapter 7) but does not include SKP sequences.
CP1	D10.2	Nyquist frequency
CP2	D24.3	Nyquist/2
CP3	K28.5	COM pattern
CP4	LFPS	The low frequency periodic signaling pattern
CP5	K28.7	With de-emphasis
CP6	K28.7	Without de-emphasis
CP7	50-250 1's and 0's	With de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP8	50-250 1's and 0's	With without de-emphasis. Repeating 50-250 1's and then 50-250 0's.
CP9		Pseudo-random data pattern (see section 6.4.4.1)
CP10	AAh	Nyquist pattern at 10Gb/s. This is not 128b132b encoded.
CP11	CCh	Nyquist/2 at 10Gb/s, This is not 128b132b encoded.
CP12	LFSR15	Uncoded LFSR15 for PHY level testing and fault isolation. This is not 128b132b encoded.

Note: Unless otherwise noted, scrambling is disabled for compliance patterns.







- **LFPS, CP9,CP10 are used for Compliance testing for TX**
- CP0 through CP8 are transmitted at Gen 1 rate, while **CP9 through CP12 are transmitted at Gen 2 rate.**
- Gen 2 compliance pattern comprises a pseudo-random data pattern
- The pattern repeats every 65536 symbols and starts with a SYNC Ordered Set

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LFPS plus Encoding for USB3.1

- LFPS

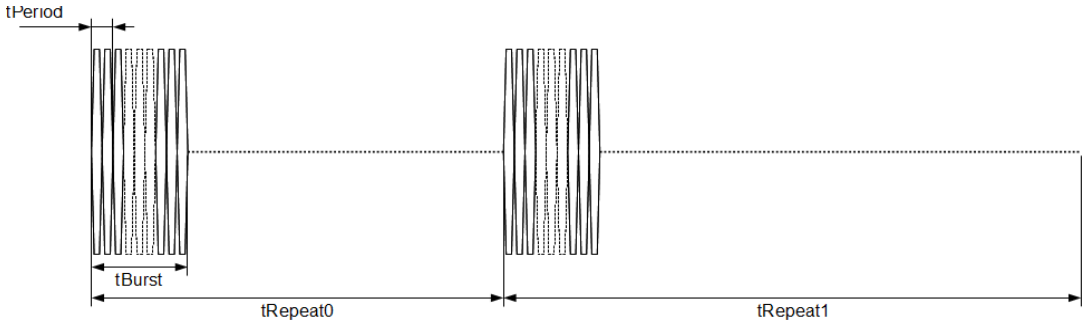
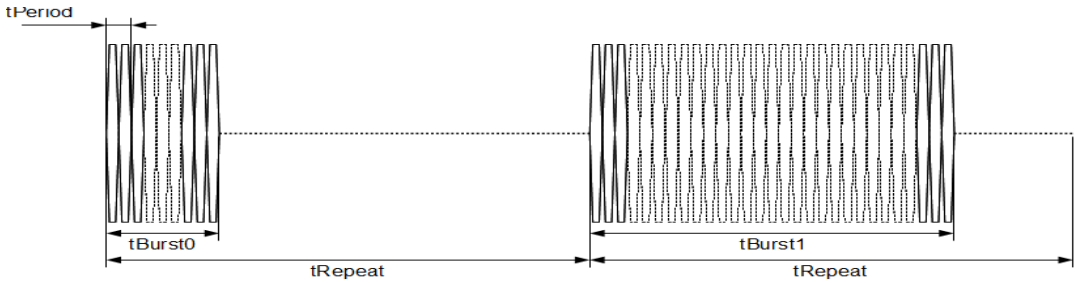


Table 6-31. Binary Representation of Polling.LFPS

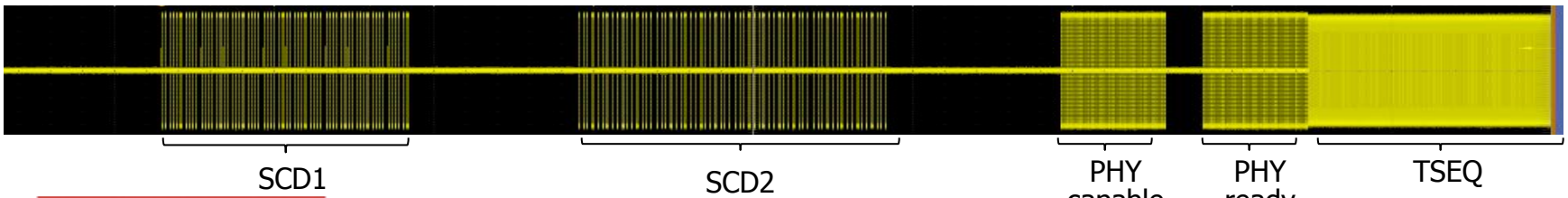
tRepeat (us)	Logic value
6~9	'0'
11~14	'1'
9~11	illegal

- SuperSpeed+ identity check
- tRepeat Modulation
- SCD1.LFPS (4'b0010)
- SCD2.LFPS (4'b1101)

- LFPS Based PWM Signaling (LBPM)



- Rate (speed and lane) announcement and negotiation
- Repeater declaration
- Power state transition in repeater



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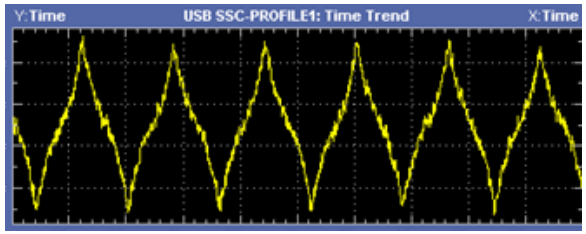
USB 3.1 Transmitter Measurement Overview

Spec Reference	Parameter
Table 6-16	SSC Modulation Rate SSC Deviation
Table 6-17	Unit Interval including SSC Maximum Slew Rate (5 GT/s) SSC df/dt (10 GT/s)
Table 6-17	Differential p-p Tx Voltage Swing Low-power Differential p-p Tx Voltage Swing De-emphasized Output Voltage Ratio (5 GT/s)
Table 6-18	Tx Min Pulse Deterministic Min Pulse Transmitter DC Common Mode Voltage Tx AC Common Mode Voltage Active
Table 6-19	Transmitter Eye RJ/DJ/TJ - Dual Dirac at 10–12 BER
Table 6-28	LFPS Common Mode Voltage LFPS Differential Voltage LFPS Rise Time LFPS Fall Time LFPS Duty Cycle LFPS tPeriod LFPS tPeriod-SSP (10 GT/s)
Table 6-29	LFPS tBurst LFPS tRepeat
Table 6-31	LFPS tRepeat-0 (10 GT/s) LFPS tRepeat-1 (10 GT/s)
Table 6-32	LFPS Pulse Width Modulation (10 GT/s) tLFPS-0 (10 GT/s) tLFPS-1 (10 GT/s)

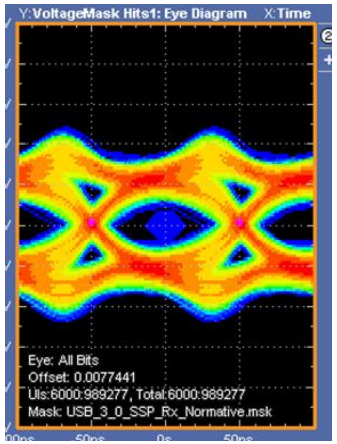
Clock

(CP10)

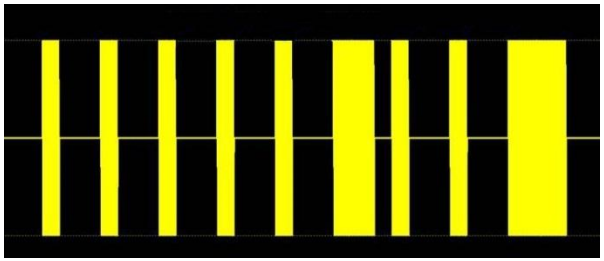


PHY

(CP9)*



LFPS



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USB3.1 Transmitter Compliance Testing

1. Connect DUT to scope via test fixture.
2. Transmit CP10 (clock) & measure 10^6 consecutive UI
   - This step used to measure RJ
   - Requires toggling from default CP0 up to CP10
3. Repeat with CP9 (scrambled data pattern)
   - Will combine RJ (step 2) with DJ to extrapolate TJ (step5)
4. Post-process the waveforms with the compliance channel, the reference CTLE, & jitter transfer function
   - Channels are S-Parameter-based and are embedded into captured waveform
5. Extrapolate jitter to 10^{-12} BER

Spec	Min	Max	Units
Eye Height	70	1200	mV
Dj @ 10^{-12} BER		0.530	UI
Rj @ 10^{-12} BER		0.184	UI
Tj @ 10^{-12} BER		0.714	UI

USB3.1Transmitter Compliance Testing

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CP9		Pseudo-random data pattern (see section 6.4.4.1)
CP10	AAh	Nyquist pattern at 10Gb/s. This is not 128b132b encoded.
CP11	CCh	Nyquist/2 at 10Gb/s, This is not 128b132b encoded.
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Note: Unless otherwise noted, scrambling is disabled for compliance patterns.

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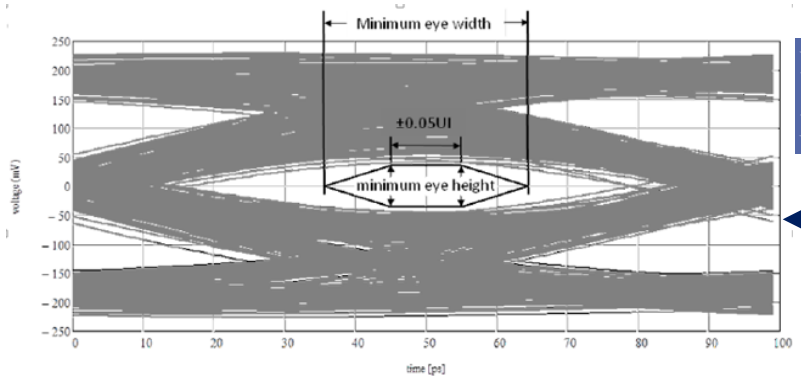
- Gen 2 compliance pattern comprises a pseudo-random data pattern
- The pattern repeats every 65536 symbols and starts with a SYNC Ordered Set



Gen 2 eye mask

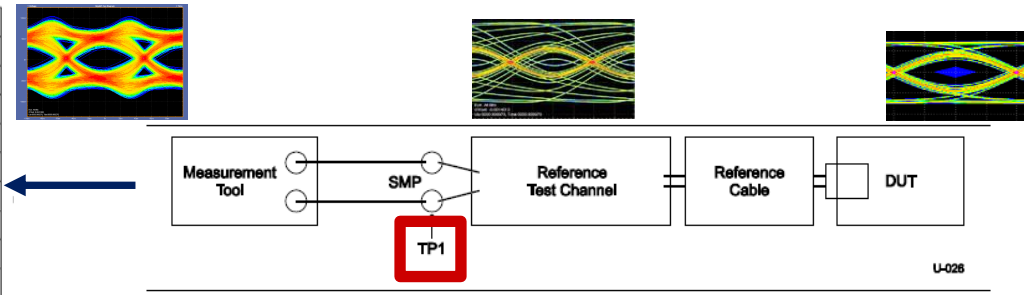


Figure 6-19. Tx Normative Setup with Reference Channel

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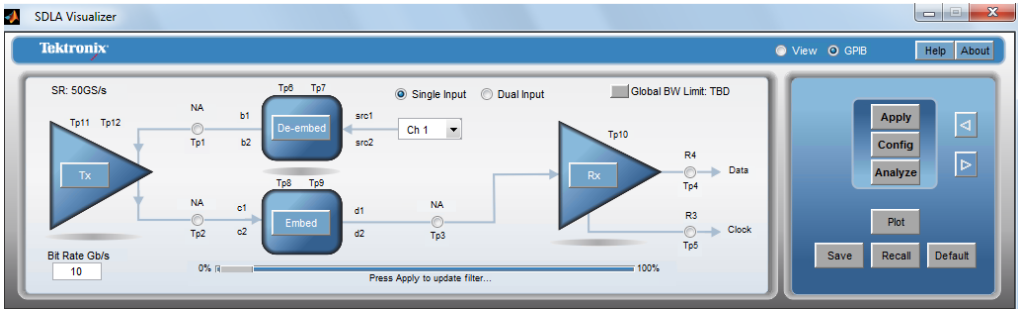
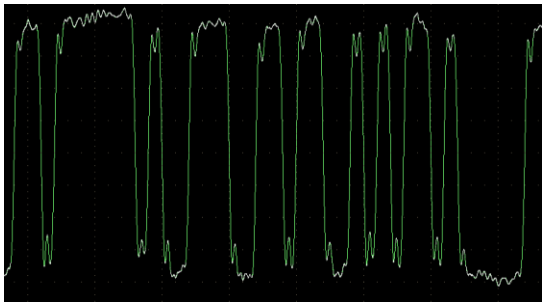
Transmitter Capture and Channel Embed

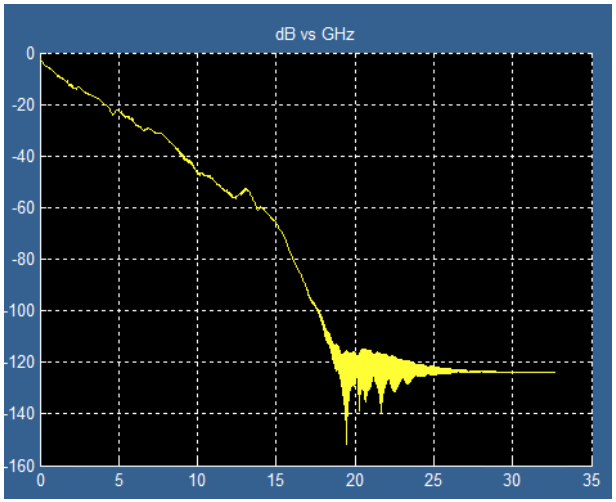
- Capture CP9 (data) and CP10 (clock)
- Input reference channel models

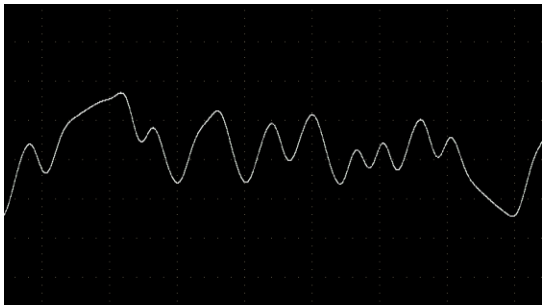




CP9 Scrambled Pattern (TP0)

Reference Channel





CP9 Scrambled Pattern (TP1)

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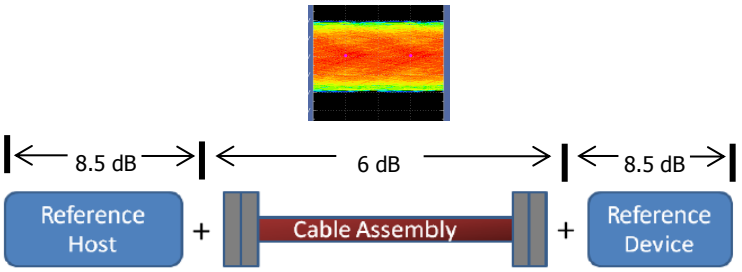
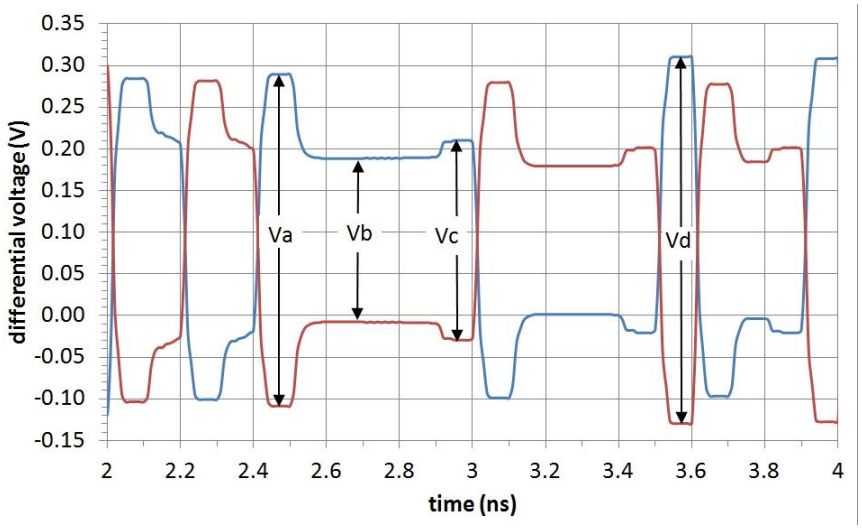
Reference Tx Equalization

- USB channel profiles are dynamic (consumer)
- Need flexible solution space for link optimization
- Below are recommended Tx settings for good margin with target reference channels

Host/Device Loss	<3.5dB	≥3.5dB
C_{-1}	0.000	-0.125
C_1	-0.100	-0.125
Va/Vd	1.00	0.80
Vb/Vd	0.75	0.55
Vd/Vd	0.75	0.75





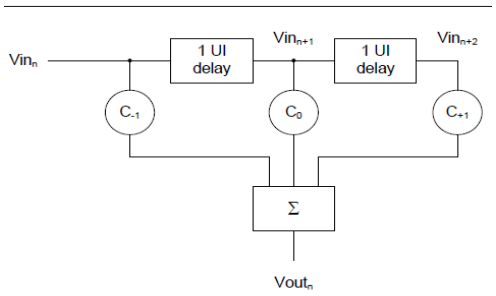
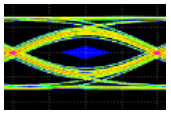


Figure 6-21. 3-tap Transmit Equalizer Structure



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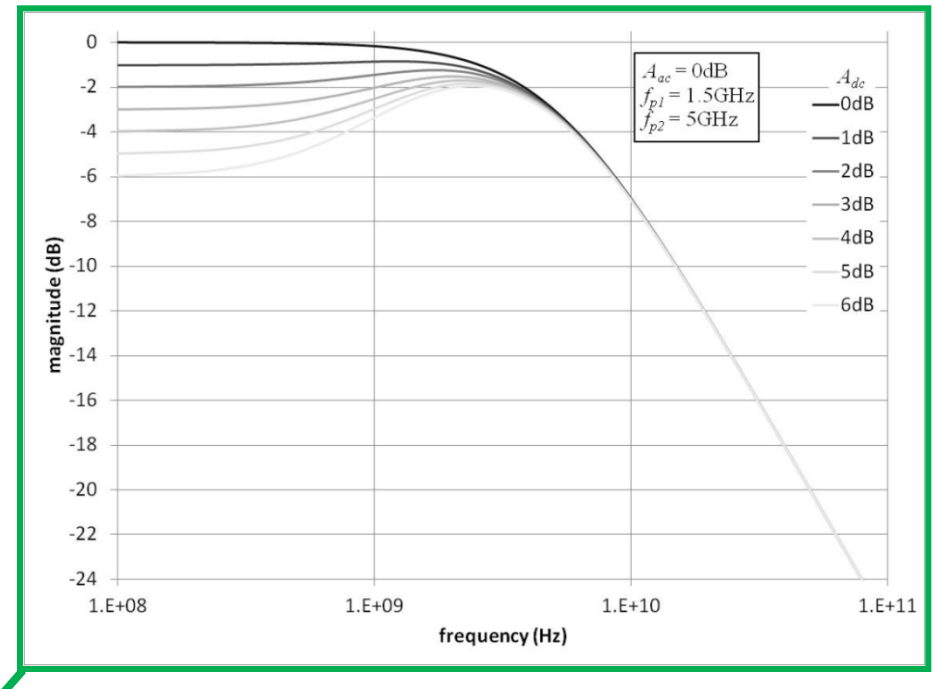
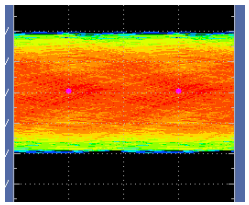
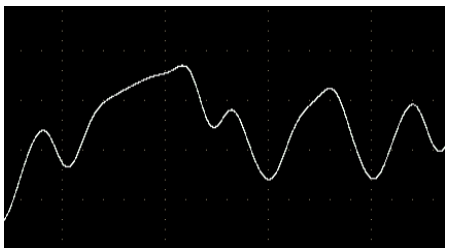
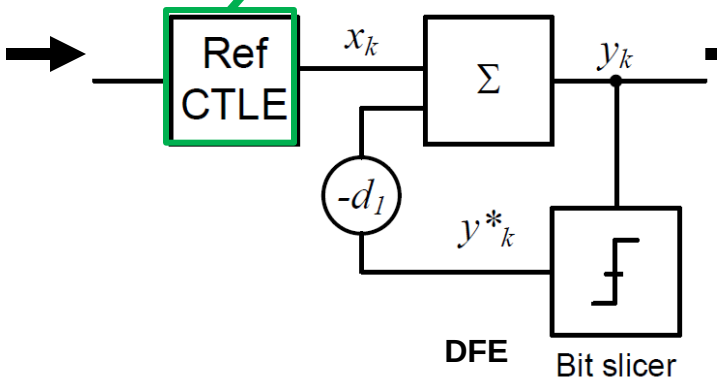
Reference RX Equalizer

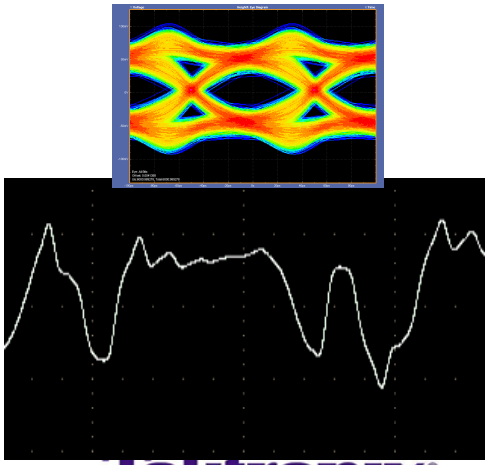
- Far End (TP1) Eye closed
- Need to open eye with EQ
- Adaptation only for Rx
  - No back channel Tx negotiation
- Iterate through multiple CTLE gain settings + 1-tap DFE











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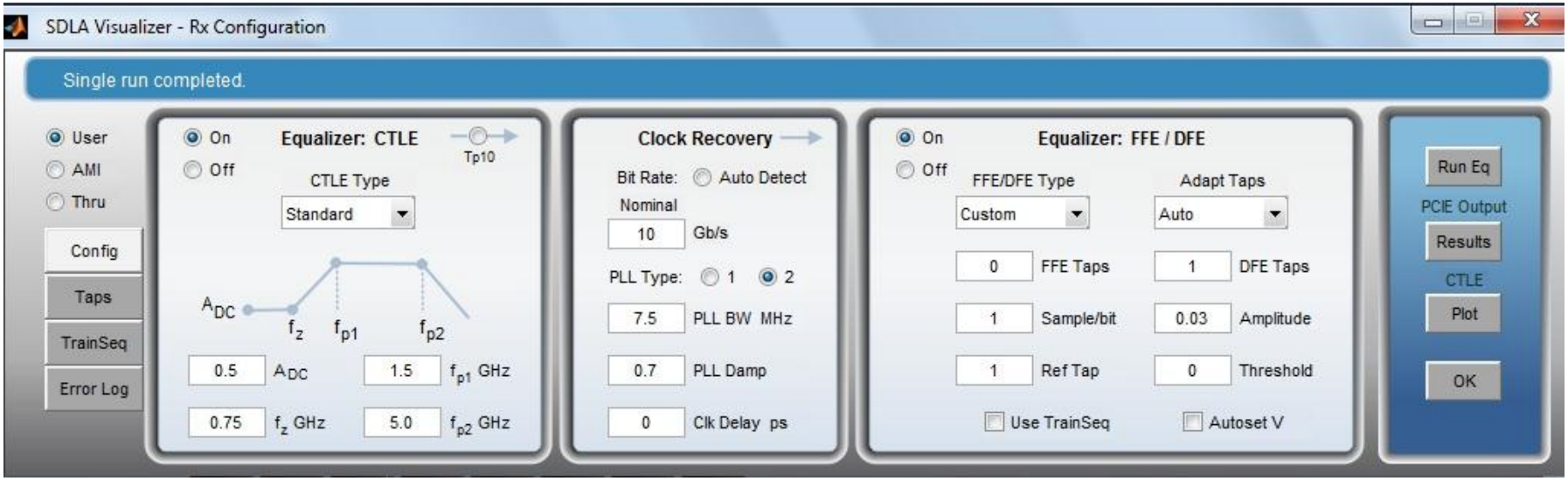
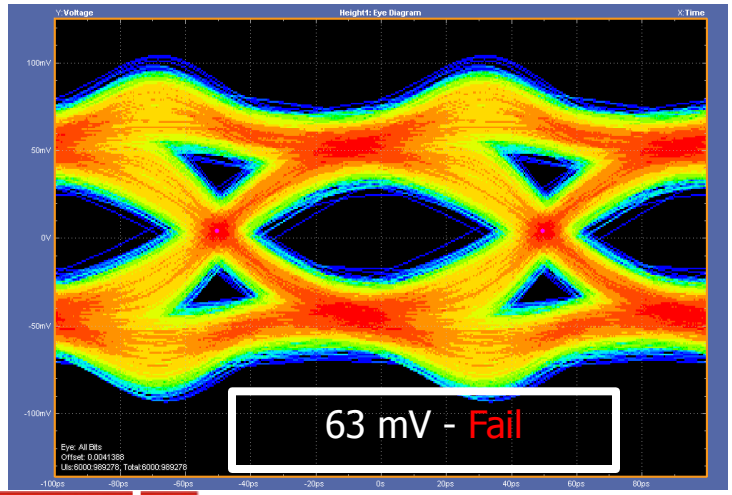
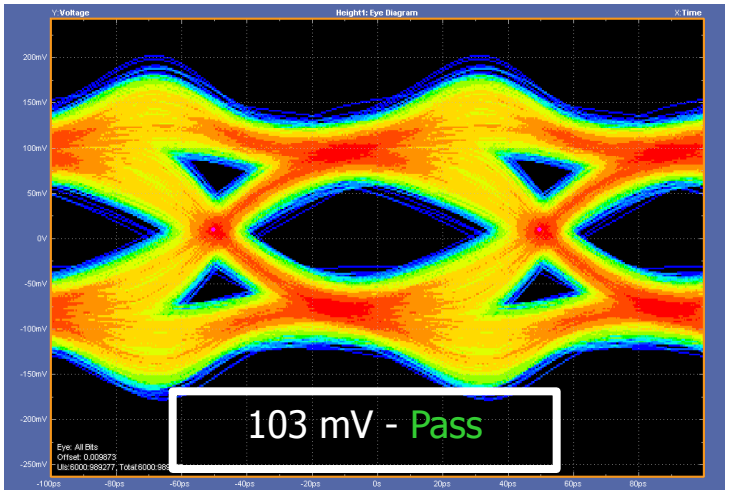
Transmitter Validation Example

- Find optimum Eye height vs. Rx EQ –CTLE and DFE







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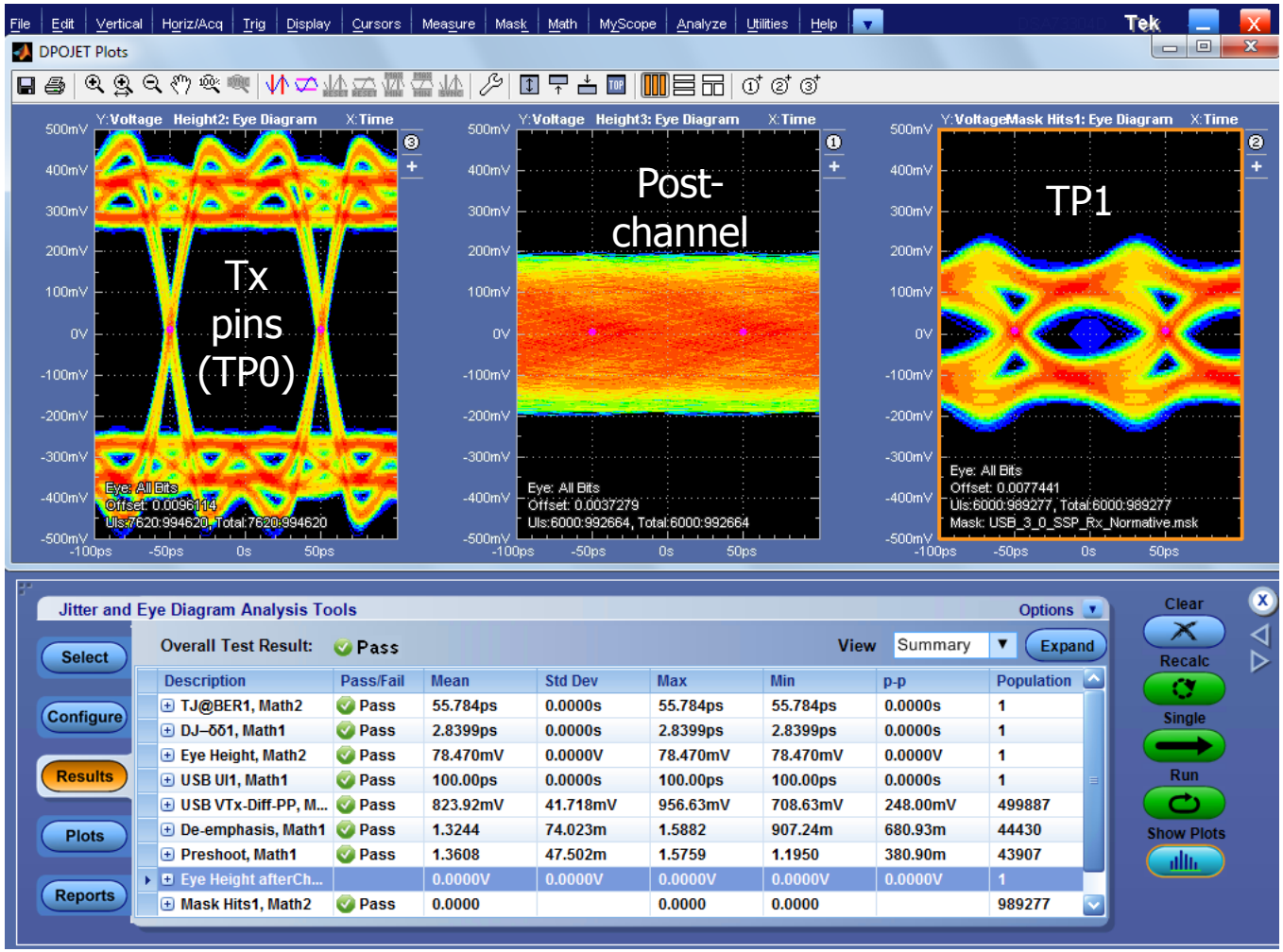
Transmitter Validation Example - DPOJET

- Measure Eye height and jitter at TP1



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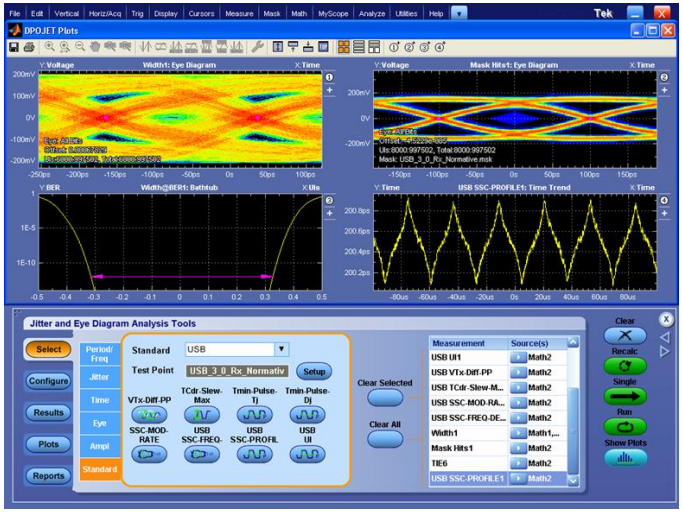
TekExpress USBSSP-TX Software

- Automates USB 3.1 gen1 & gen2 electrical tests
- Built-in control of LFPS generator for pattern toggle
  - CP0 – CP12
- Use preferred operating mode for your application
  - **Compliance:** Full automation of ping.LFPS, analysis and reporting
  - **User-defined:** Custom channel characterization and test limits
  - **Debug:** DPOJET based manual measurements with expanded jitter analysis and plotting capabilities



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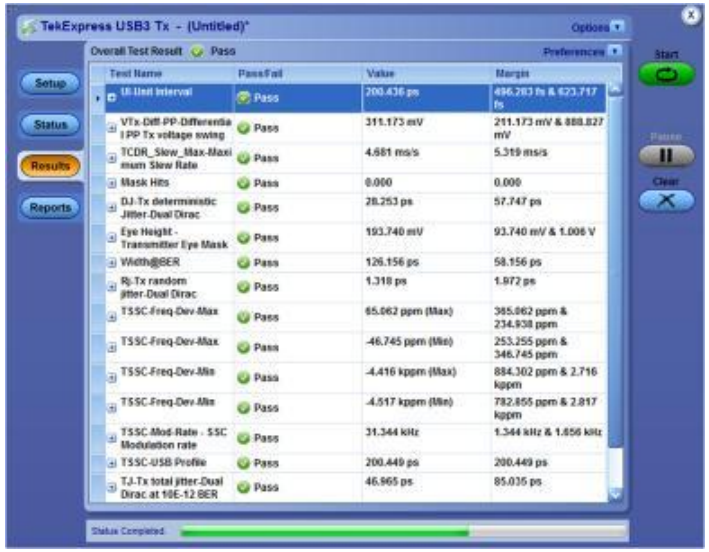
USB 3.1 Recommended Transmitter Solution

- ≥ 23 GHz BW, 100 GS/sec preferred
- >10M minimum record length allows capture of 1M UI at 100 GS/sec, no interpolation.
- DPOJET for advanced jitter/eye analysis (Option DJA)
- SDLA for channel embedding and cycling through 7 CTLE/1 DFE settings (Option SDLA64)
- TekExpress automation software for USB 3.1 gen1/gen2 physical layer validation (Option USBSSP-TX)



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Receiver Compliance Test

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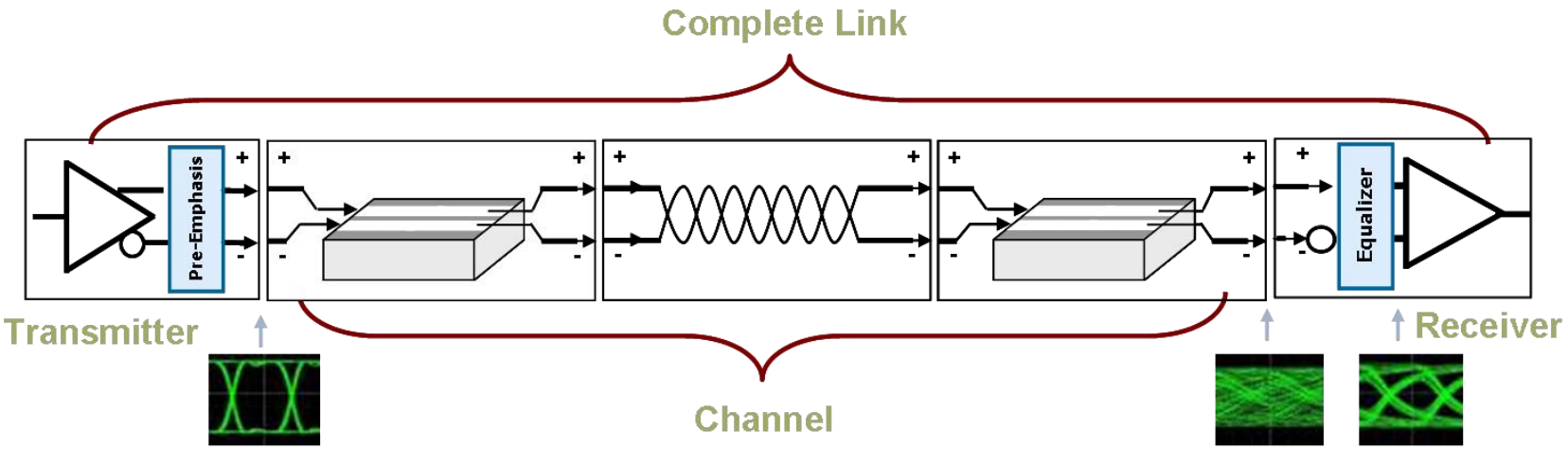
USB 3.1 Receiver Testing Overview

- A jitter tolerance test is required for certification, though debug and characterization capabilities are needed to ensure that receivers will work in real world conditions
  - Send specific test data patterns to the device-under-test (DUT) through a known channel (fixtures and cables)
  - Add a specific “recipe” of stresses and de-emphasis
  - Command the DUT into loopback mode (far-end retimed)
  - Return “echoed” data to a BERT
  - Detected errors are inferred to be a result of bad DUT receiver decisions



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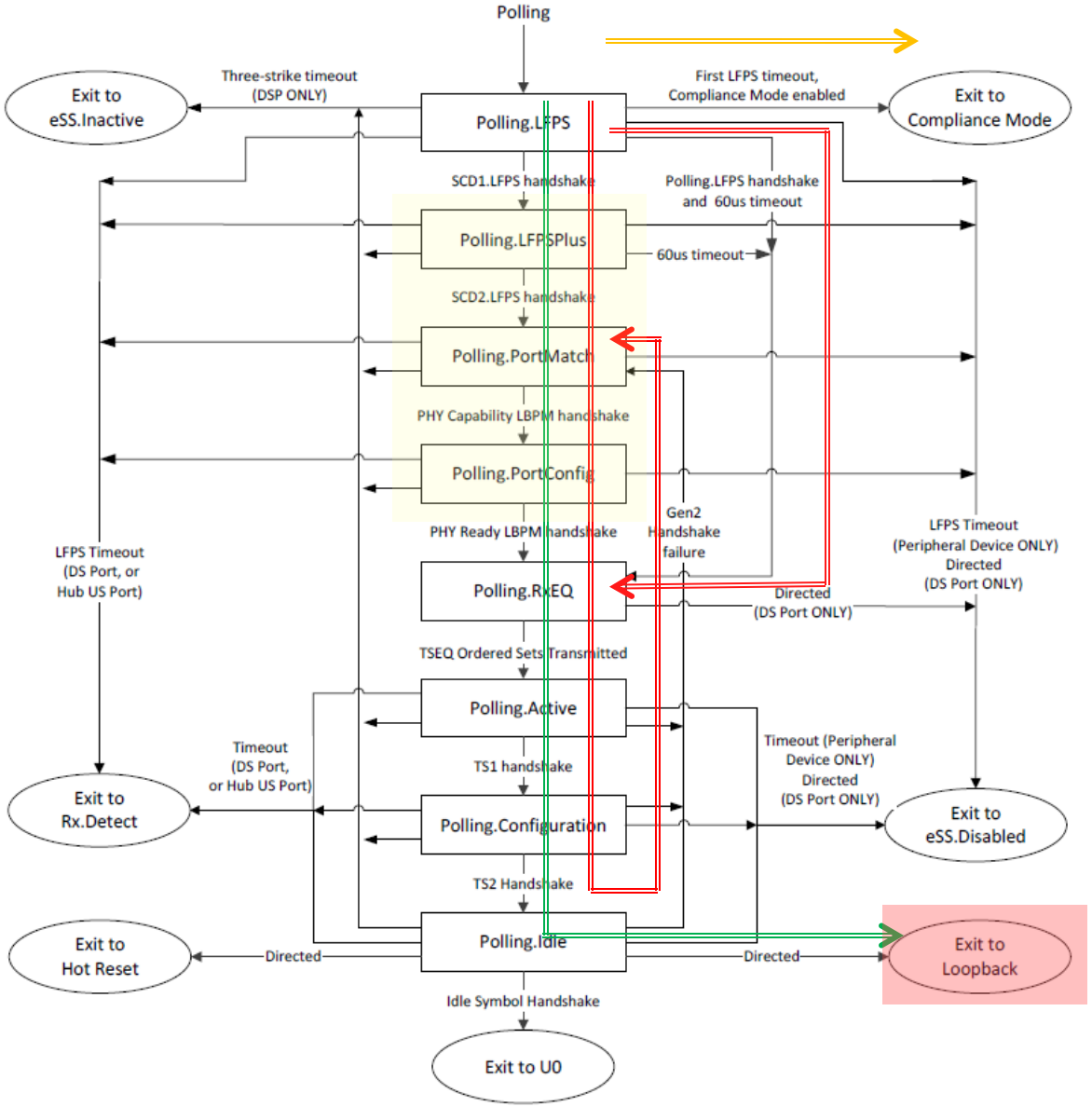
Polling Sub-states –Loopback



Successful Gen2 link training with loopback asserted – Enter in Loopback mode

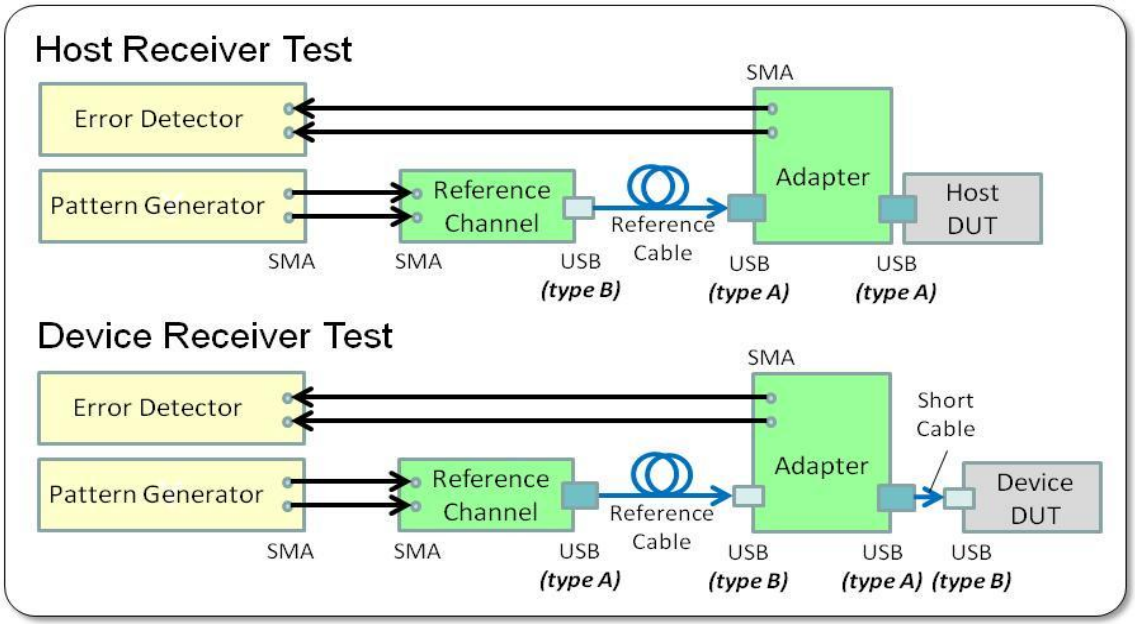
No link partner response – Enter Tx compliance mode

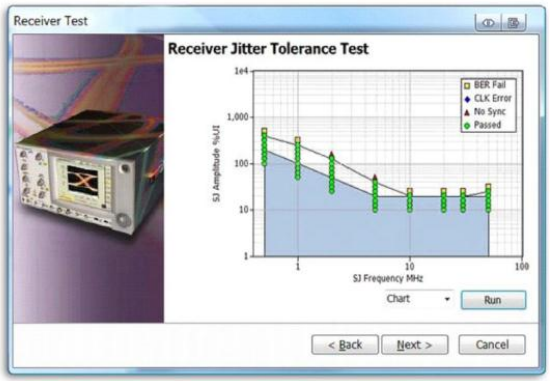
Training failure – Retry at Gen1 rate

LFPS detected but no LFPSPlus - Train at Gen1 rate

Receiver Testing

- Jitter Tolerance (JTOL) with swept jitter profile, reference channel
  - Verify CDR tracking and ISI compensation
- Link optimization/training critical
  - No back channel negotiation
- Return “echoed” data to a BERT (loopback)
- Detected errors are inferred to be a result of bad DUT receiver decisions





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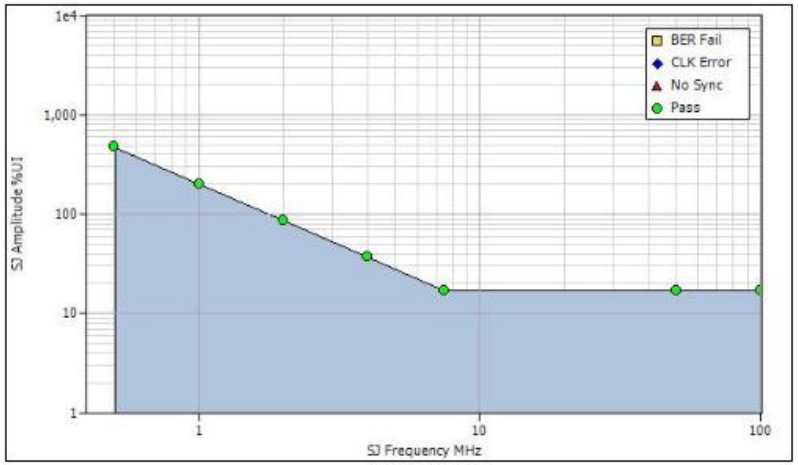
Receiver Tolerance Test Overview

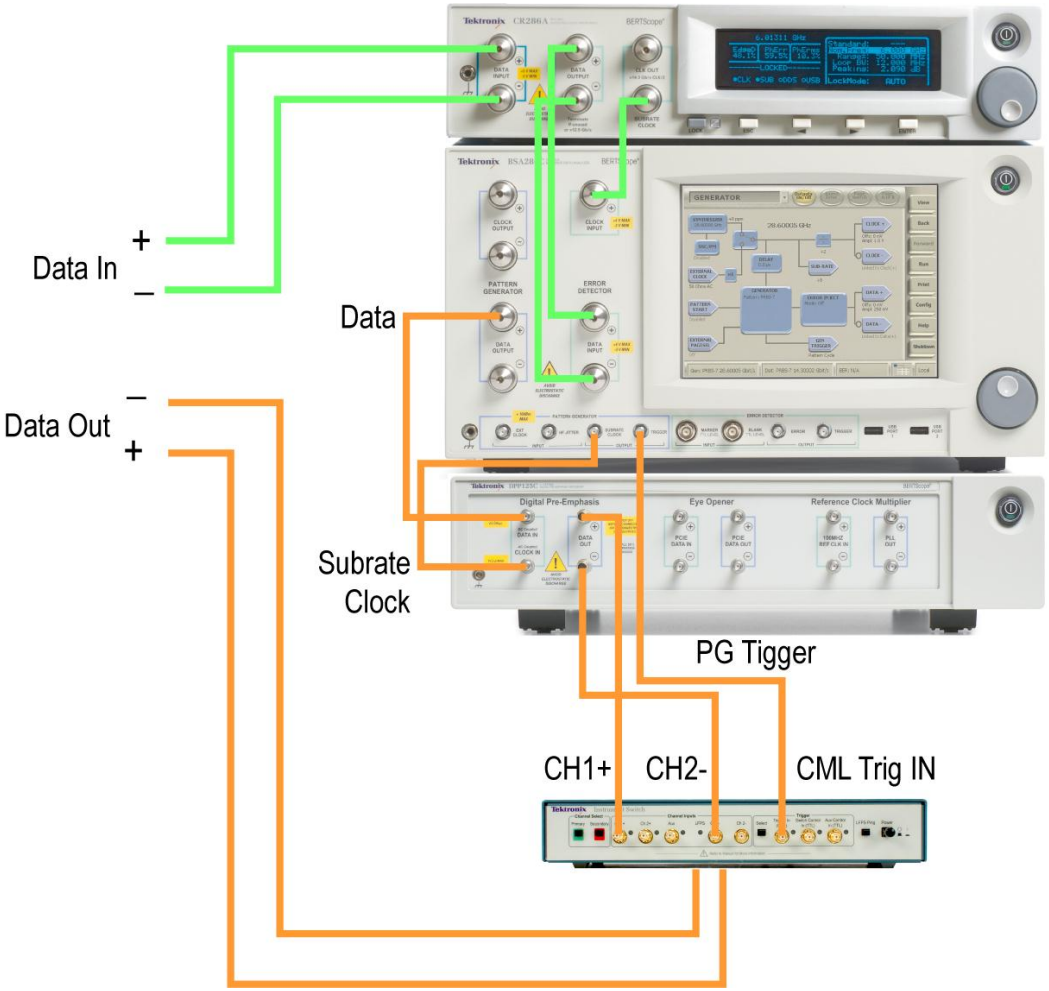
- 7Test Points
- SSC Clocking is enabled
- BER Test is performed at 10^{-10}
- Preshoot/De-emphasis enabled
- Stress verified by TJ/Eye Height
- Each SJ term in the table below is tested one at a time after the device is in loopback mode

Frequency	SJ	RJ
500kHz	476ps	1.308ps RMS
1MHz	203ps	1.308ps RMS
2MHz	87ps	1.308ps RMS
4MHz	37ps	1.308ps RMS
7.5MHz	17ps	1.308ps RMS
50MHz	17ps	1.308ps RMS
100MHz	17ps	1.308ps RMS



MHZ	Test	Template	Bits	Errors	BER	Status	Margin
0.50	476.00%	476.00%	3.00e010	0	0.00e000	Passed	0.00%
1.00	203.00%	203.00%	3.00e010	0	0.00e000	Passed	0.00%
2.00	87.00%	87.00%	3.00e010	0	0.00e000	Passed	0.00%
4.00	37.00%	37.00%	3.00e010	0	0.00e000	Passed	0.00%
7.50	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%
50.00	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%
100.00	17.00%	17.00%	3.00e010	0	0.00e000	Passed	0.00%

BERTScope USB 3.1 Receiver configuration solution



- **CR125A**
  - Clock Recovery
- **BSA125C**
  - BERTScope
- **USB3.1 automation software**
- **DPP125C**
  - De-emphasis
- **USB Switch**
  - Creates LFPS required to initiate Loopback-mode

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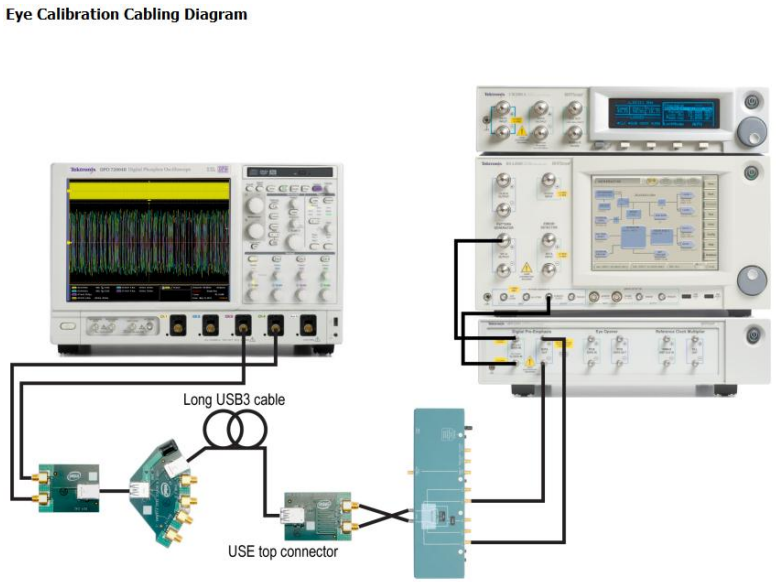
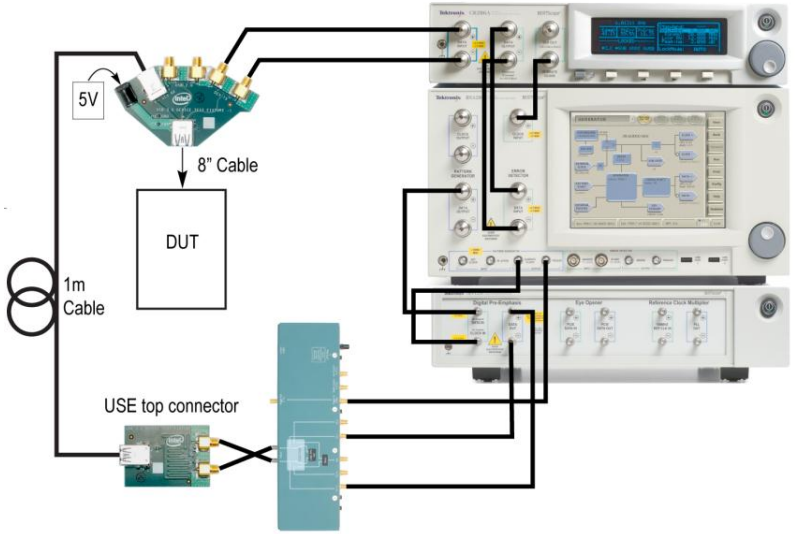
USB3.1 Rx compliance
RX testing using BERTSCOPE

- USB-IF ‘Compliance Channel
- Jitter tolerance testing using BERTSCOPE
- Auto Calibration & measurement Tools
- Powerful Jitter insertion function for Developers.



USB3.1_Rx Calibration Configuration with BERTScope



USB3.1_Rx Testing Configuration with BERTScope

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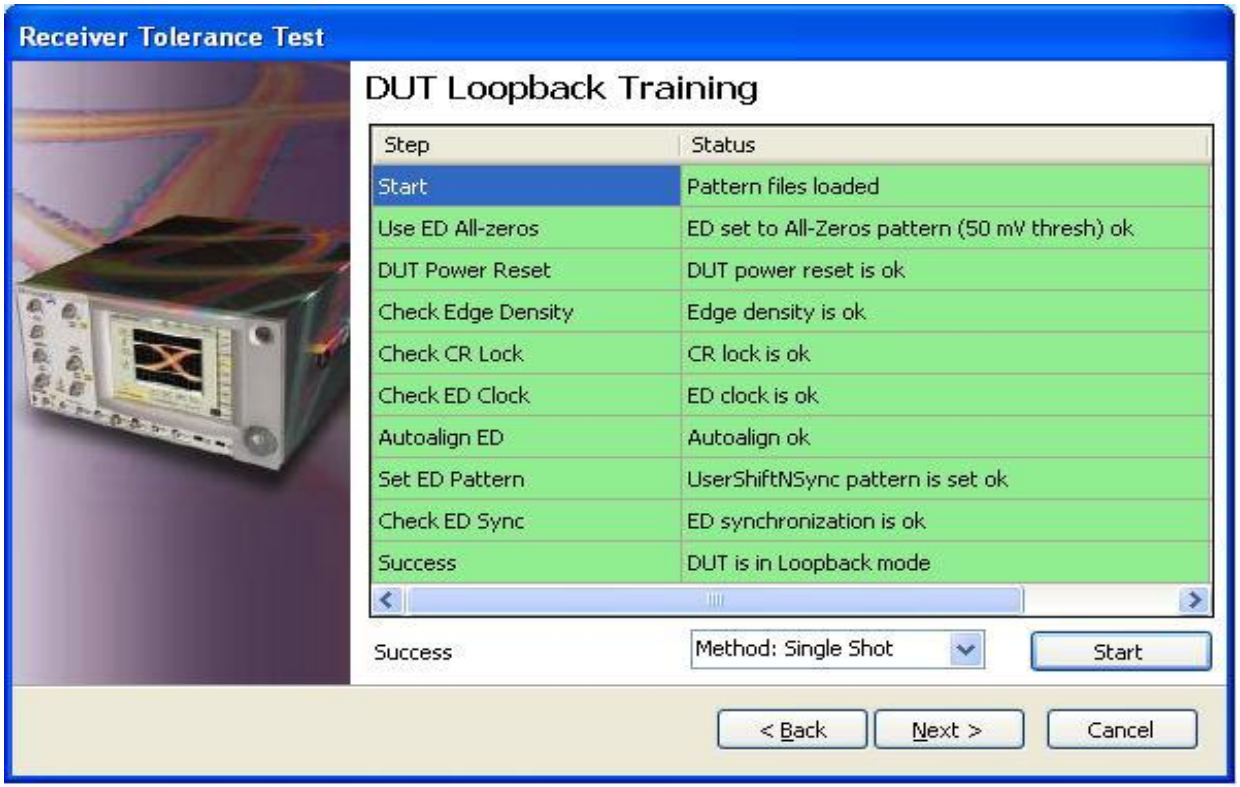
Loopback Initiation



- Loopback initiation prepares devices for receiver testing
- Automation software controls the loopback sequence, eliminating guesswork so users focus on testing and debugging

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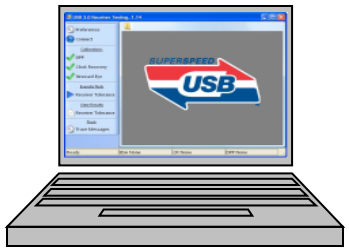
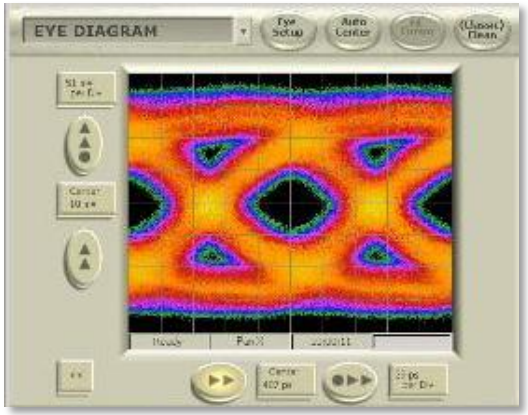
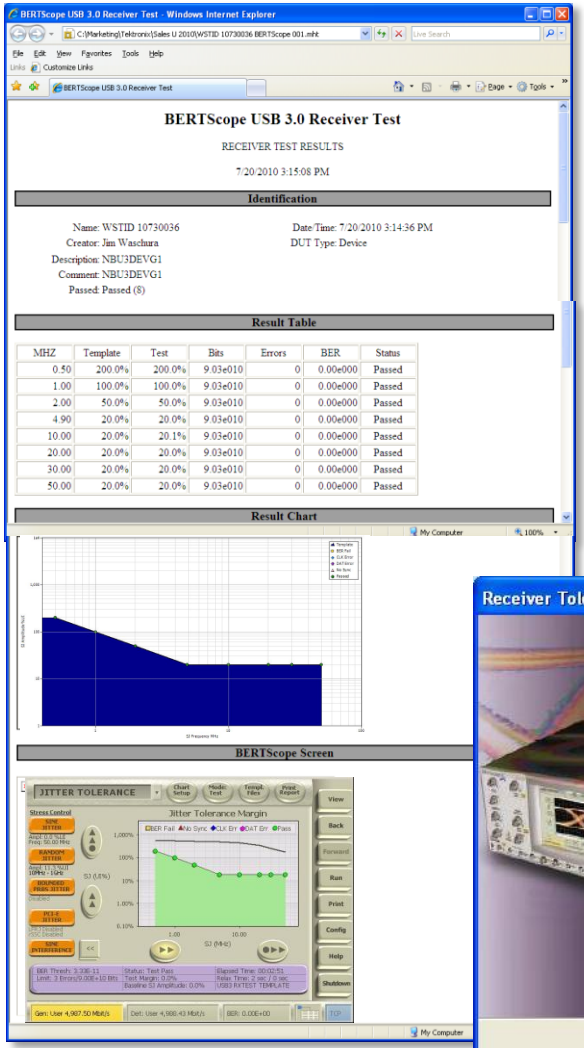
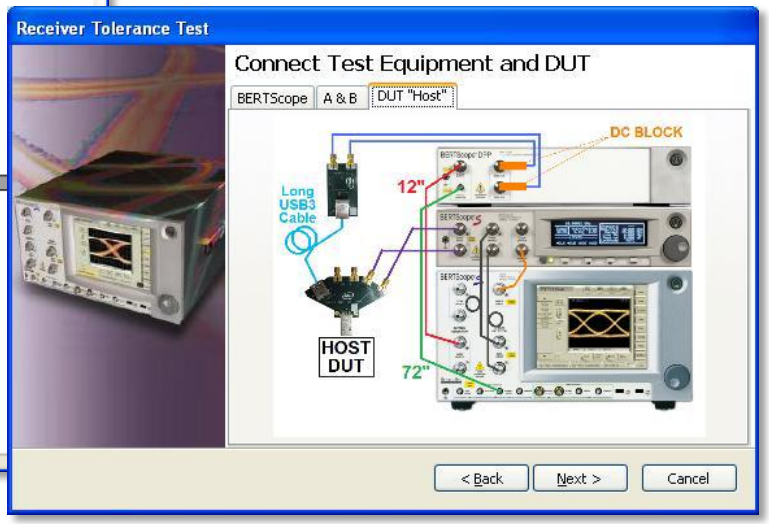
Automation Software Makes Testing Even Easier



Automation Software







- Results stored to database for easy recall and management
- HTML style test reports
- Cabling diagrams for straightforward setups
- Automated Stressed Eye Calibration

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Summary

- New opportunity for growth with USB 10 Gb/s
- Adds additional challenges beyond legacy requirements (backwards compatibility)
- Higher performance, more complex design but feasible within current infrastructure
- Extensive PHY validation tools for early designs
  - New USB SSP DPOJET setups for Tx validation
  - BERTScope USB library with JTOL templates
  - DSA8300 Sampling oscilloscope for channel characterization
  - Test procedures documented in Methods of Implementation (MOI)

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Tektronix MHL 3.2 TX,RX Solution

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MHL – CTS 3.2

- MHL Consortium and Tektronix has worked together on the 3.0 version MHL specifications.
  - **Data rate changes to 6Gbps.**
  - **MHL Clock is no longer common mode but transmitted on eCBUS**
  - eCBUS has bi-drectional ecbus data and clock
  - New test procedures for Source, Sink and Dongle
  - Most of the CTS 2.1 tests need to be used to ensure backward compatibility exists.

MHL 3.0/CTS3.2

- Signaling

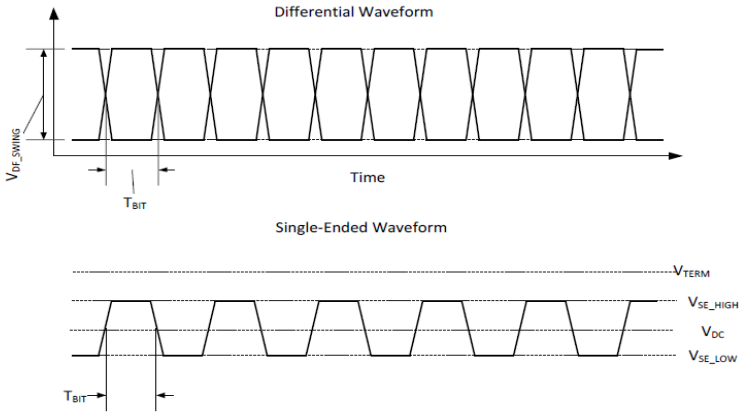

Figure 16-4. Voltage and Timing Parameters of a Differential Signal and a Single-Ended Signal

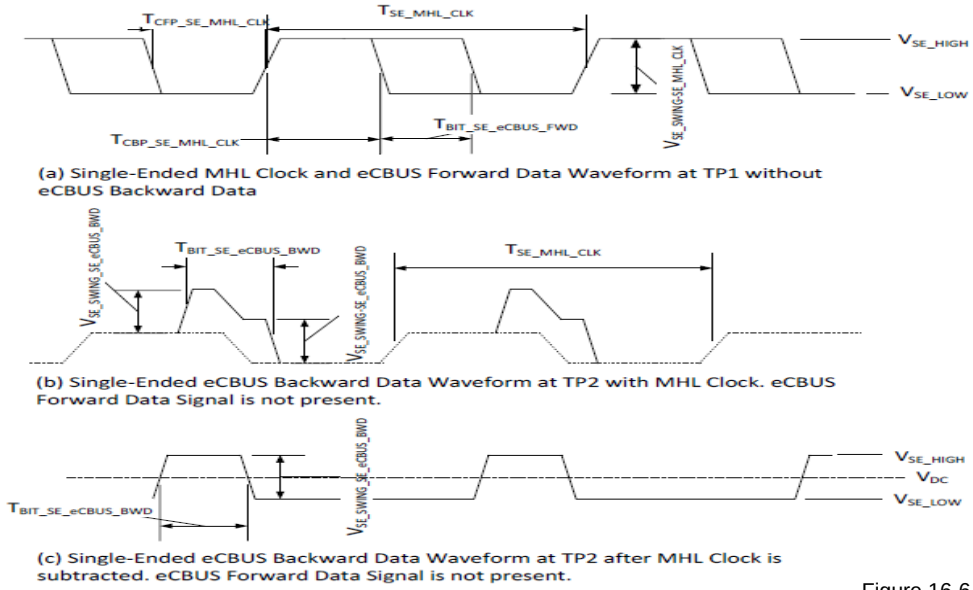

Figure 16-5. Voltage and Timing Parameters of a Single-ended MHL Clock and eCBUS Forward and Backward Signals

- VDF_SWING in Figure 16-4 represents
  - VDF_SWING_DF_TMDS_DATA
  - VDF_SWING_DF_MHL_CLK
  - VDF_SWING_DF_eCBUS_FWD
- VSE_HIGH represents
  - VSE_HIGH_DF_TMDS_DATA
  - VSE_HIGH_DF_MHL_CLK
  - VSE_HIGH_DF_eCBUS_FWD
- VSE_LOW represents
  - VSE_LOW_DF_TMDS_DATA
  - VSE_LOW_DF_MHL_CLK
  - VSE_LOW_DF_eCBUS_FWD

Figure 16-6. Voltage and Timing Parameters of a Differential MHL Clock and eCBUS Forward and Backward Signals

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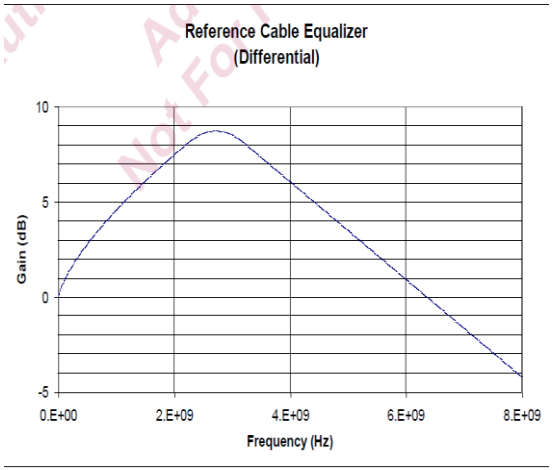
MHL 3.0/CTS3.2
- EQ and Cable Emulator

- **Reference Cable Equalizer**
  - Two reference cable equalizers are used
  - Used to produce the MHL eye diagram and clock jitter measurements at TP2 for TMDS and eCBUS forward signals,
  - Used to produce at TP1 for eCBUS backward signals

> 6Gbps reference cable equalizer
  - Shall meet the transfer function shown in Figure 16-15 (Differential)
  - Applied to the TMDS signal at the 6Gbps data rate.

> MHL 2.1 reference cable equalizer
  - Applied to 3Gbps and to 1.5Gbps TMDS signals, and to eCBUS-D signals
  - Applied to the single-ended MHL clock signal when the single-ended MHL clock signal is tested for clock jitter, TMDS eye diagram, and eCBUS-S data eye diagram tests.

- **Worst Case Cable Emulator**
  - The worst case cable emulator is used to perform TP2 tests for TMDS, eCBUS Forward signals and TP1 tests for eCBUS Backward signal



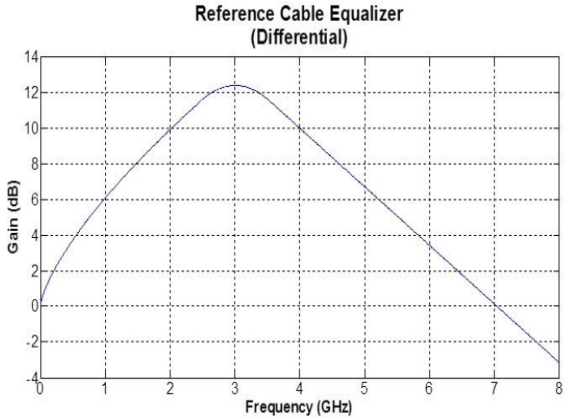


Figure 16-15. 6Gbps Reference Cable Equalizer Gain Curve

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Tektronix MHL 3.2 CTS Tx Solution- Test Details

DUT	Type	TEST	
MHL Source	Output	3.7.2.1	Single-Ended high level output voltage: Differential TMDS Data+/-
		3.7.2.2	Single-Ended low level output voltage: Differential TMDS Data+/-
		3.7.2.5	Differential output swing voltage: Differential TMDS Data
		3.7.2.7	Single-Ended high level output voltage: Single-Ended MHL CLK, Single-Ended eCBUS Forward
		3.7.2.8	Single-Ended low level output voltage: Single-Ended MHL CLK, Single-Ended eCBUS Forward
		3.7.2.9	Single-Ended output swing voltage: Single-Ended MHL CLK, Single-Ended eCBUS Forward
		3.7.2.13	Rise Time, Differential TMDS Data
		3.7.2.14	Fall Time, Differential TMDS Data
		3.7.2.17	Peak-Peak Amplitude: Differential TMDS Data
		3.7.2.20	Single_Ended MHL Clock Frequency
		3.7.2.23	Rise Time: Single-ended MHL Clock
		3.7.2.24	Fall Time: Single-ended MHL Clock, Single-ended eCBUS Forward
		3.7.7.25	Peak-Peak Amplitude, eCBUS-S Forward
		3.7.7.26	Single-Ended MHL Clock Jitter
		3.7.7.27	MHL3 Differential Eye Diagram Mask at TP2 for TMDS Data
		3.7.2.29	MHL3 Single-ended Eye Diagram Mask at TP2 for Single-Ended eCBUS FWD Data
	Input	3.7.2.33	Single-Ended input swing voltage: Single-Ended eCBUS Backward
		3.7.2.36	MHL3 Single-Ended Eye Diagram Mask at TP1 for Single-Ended eCBUS BWD Data
	Impedance	3.7.2.37	TMDS+ and TMDS- Differential Impedance through Connections
			TMDS+ and TMDS- Differential Impedance at Termination
		3.7.2.39	eCBUS Single-Ended Impedance through Connections
			eCBUS Single-Ended Impedance at Termination

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Tektronix MHL 3.2 CTS Rx Solution- Test Details

DUT	Type	TEST	
MHL Sink	Input	4.7.2.3	Differential input swing voltage: Differential TMDS Data
		4.7.2.6	Single-Ended input swing voltage: Single-Ended MHL CLK, Single-Ended eCBUS Forward
		4.7.2.7	Differential Intra-Pair Skew: Differential TMDS Data +/-
		4.7.2.10	Jitter Tolerance of Single-Ended MHL CLK, eCBUS-S FWD Data and Differential TMDS Data
	Output	4.7.2.14	Single-Ended high level output voltage:Single-Ended eCBUS Backward
		4.7.2.15	Single-Ended low level output voltage:Single-Ended eCBUS Backward
		4.7.2.16	Single-Ended output swing voltage:Single-Ended eCBUS Backward
		4.7.2.20	Rise time, Single-Ended eCBUS Backward
		4.7.2.21	Fall Time, Single-Ended eCBUS Backward
		4.7.2.22	Peak-peak Amplitude, eCBUS-S Backward
		4.7.2.24	MHL3 Eye Diagram Mask at TP1 for Single-Ended eCBUS Backward Data
	Impedance	4.7.2.25	TMDS+ and TMDS- Differential Impedance through Connections
			TMDS+ and TMDS- Differential Impedance at Termination
		4.7.2.27	eCBUS Single-Ended Impedance through Connections
			eCBUS Single-Ended Impedance at Termination

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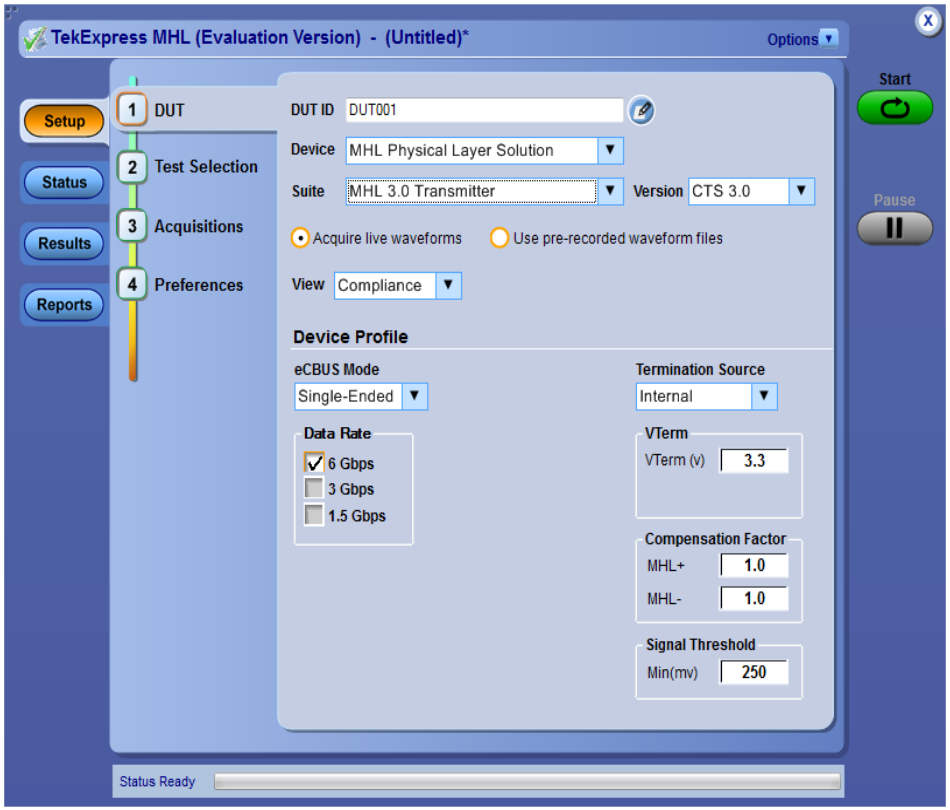
Tektronix MHL 3.2 CTS Transmitter/Receiver Solution

Transmitter Tests

- AV Link Data tests(TMDS)
- Clock Tests
- eCBUS FWD Tests
- eCBus BWD Tests

ReceiverTests

- SJT
- Intra pair skew
- eCBUS FWD Tests
- eCBus BWD Tests



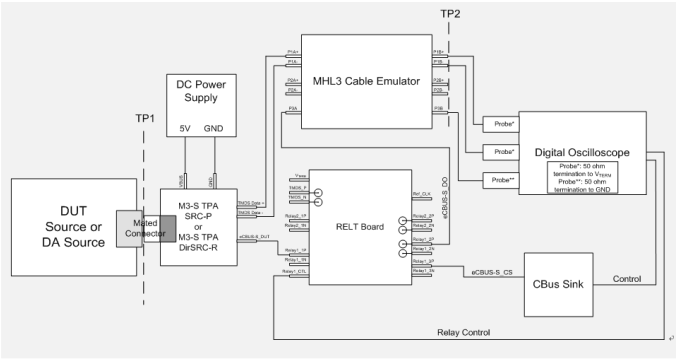


Figure 3-2. Test configuration at TP2 for source TMDS output and eCBUS-S FWD output

HDMI2.0 TX,RX Solution

–High Definition Multimedia Interface

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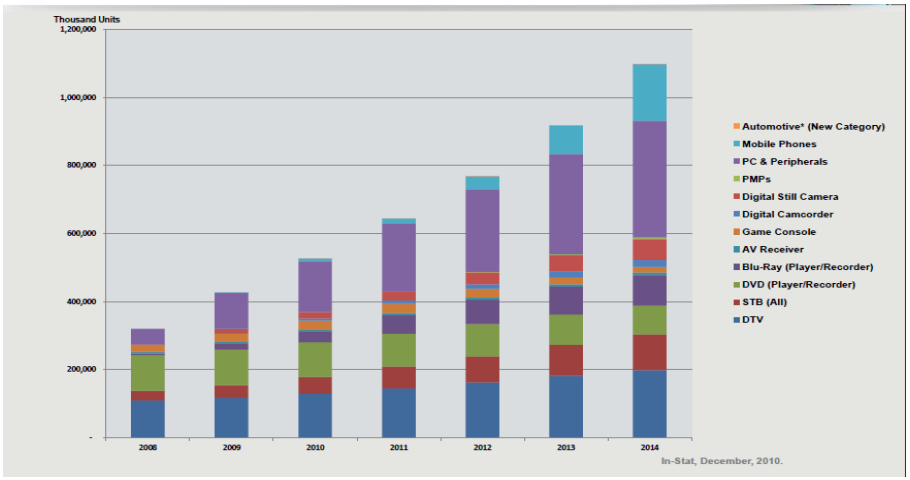
Proposed HDMI 2.0 features change

- Uses same Cat 2 Cable and HDMI 1.4b connector
- Support 4K 2K 4:4:4 60 Hz – 594Mhz
- Support 4K 2K 4:2:0 – 297Mhz
- Direct Attach device support
- Low level Bit error rate testing
- Scrambling is likely to be introduced for rates >340Mcps.



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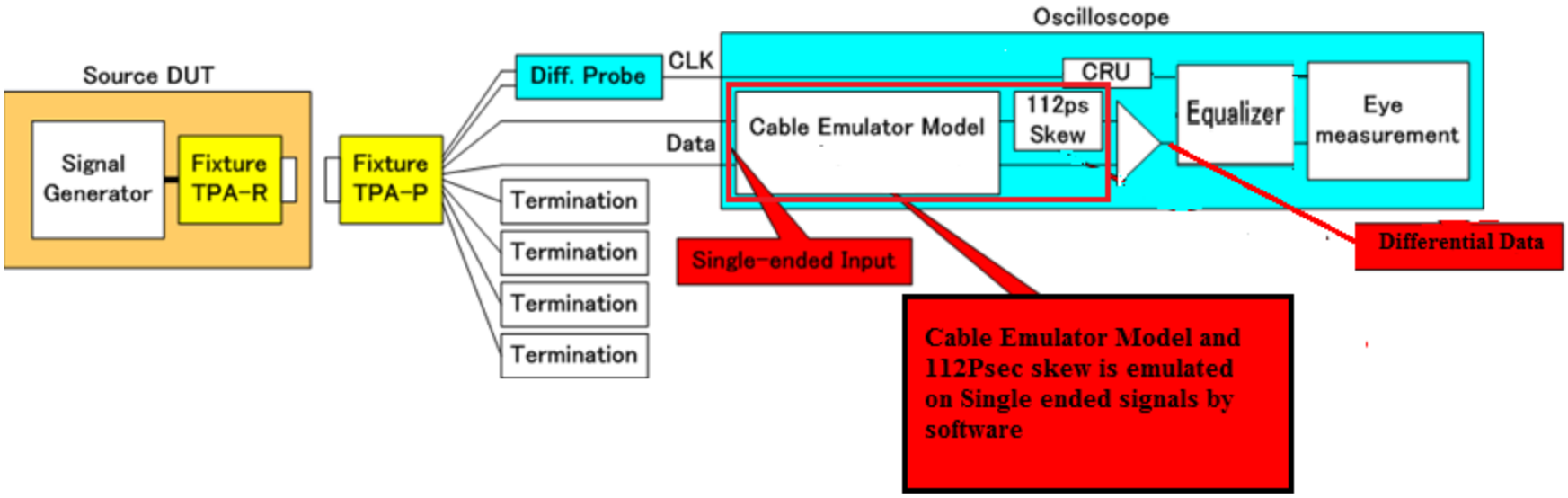
Source Testing (1.4b Vs 2.0)

- Most Source tests are likely to be same as HDMI 1.4b but for Eye Diagram test.
- Source Eye Diagram test is measured at TP2_EQ with Single ended testing
- TP2 is the signal after passing along a worst cable.
  - Worst cable has worst attenuation and skew of 112ps.
- Min 8GHz scope to 16GHz scope
- Fixtures and Probes



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Likely Source Electrical tests

Test ID HF1-1: Source TMDS Electrical – 340-600Mcsc – V_L

Test ID HF1-2: Source TMDS Electrical – 340-600Mcsc – T_{RISE}, T_{FALL}

Test ID HF1-3: Source TMDS Electrical – 340-600Mcsc – Inter-Pair Skew

Test ID HF1-4: Source TMDS Electrical – 340-600Mcsc – Intra-Pair Skew

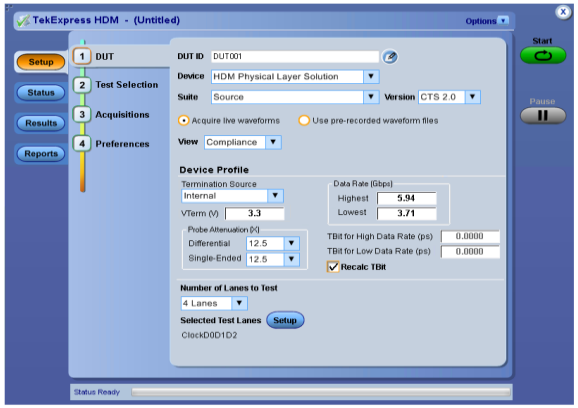
Test ID HF1-5: Source TMDS Electrical – 340-600Mcsc – Differential Voltage

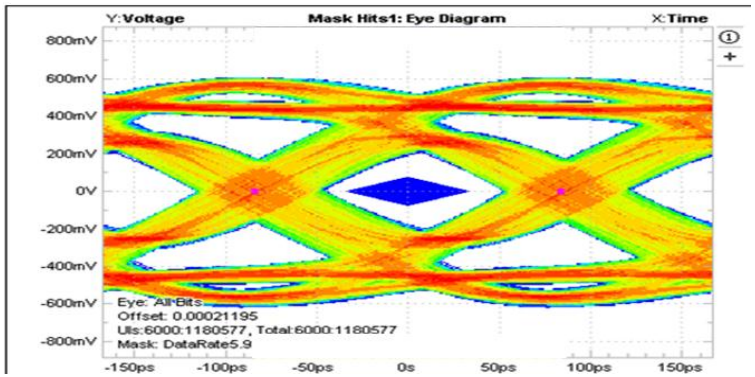
Test ID HF1-6: Source TMDS Electrical – 340-600Mcsc – Clock Duty Cycle

Test ID HF1-7: Source TMDS Electrical – 340-600Mcsc – Clock Jitter

Test ID HF1-8: Source TMDS Electrical – 340-600Mcsc – Data Eye Diagram

Test ID HF1-9: Source TMDS Electrical – 340-600Mcsc – Differential Impedance





TP2 Source Eye for HDMI 2.0 6G signal

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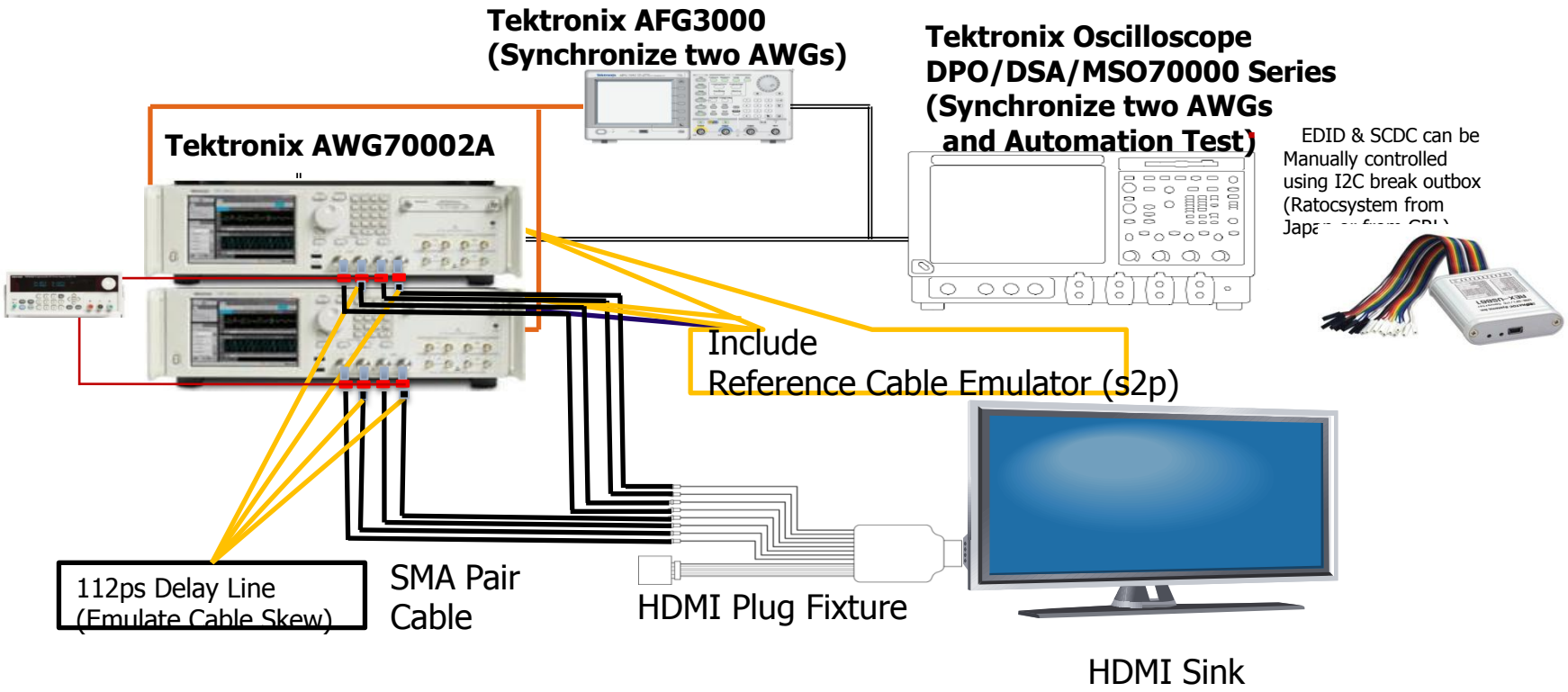
HDMI 2.0 Sink Test setup –Direct Synthesis

- **Test ID HF2-1: Sink TMDS Electrical – 340-600Mcsc – Min/Max Differential Swing Tolerance**
- **Test ID HF2-2: Sink TMDS Electrical – 340-600Mcsc – Intra-Pair Skew**
- **Test ID HF2-3: Sink TMDS Electrical – 340-600Mcsc – Jitter Tolerance**
- **Test ID HF2-4: Sink TMDS Electrical – 340-600Mcsc – Differential Impedance (performed using sampling scope)**



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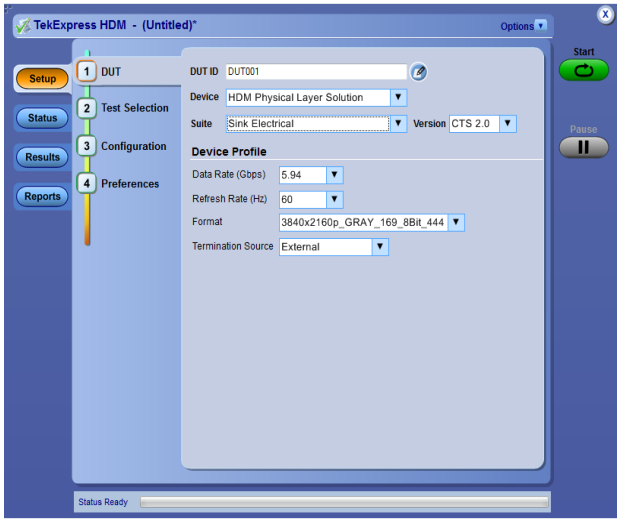
Source Sink Testing 1.4b Vs 2.0

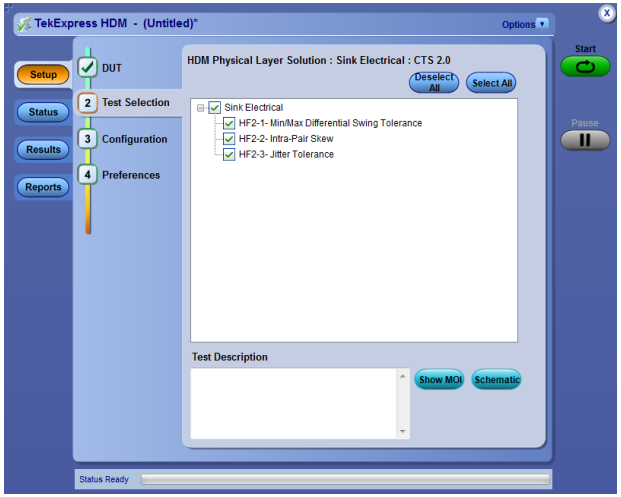
SOURCE

- DPO/DSA /MSO 70164C/D with 10XL-Minimum 16GHz BW
- Opt HDM
- Opt HT3 for 1.4 testing.
- HDMI 2.0 Fixture set(Bitifeye for now later will add Wilder)
- P7313SMA probes –Quantity 4

SINK

- Jitter Tolerance test needs +ve and –ve lanes tested with 112ps delay line
- Rest of the tests is similar to HDMI 1.4b tests
- 1.4b CTS test is a pre-requisite for HDMI 2.0
- Need AWG 70002A for HDMI 2.0 Compliance and Margin needs while AWG7122C is suitable for HDMI 2.0 Compliance testing only..
- Min 8GHz scope to 16GHz scope
- Fixtures and Probes
- HDM and HDM-DS Software (TekExpress Based)





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